BOS1211 Scalable Piezo Haptic Controller with Waveform Synthesizer

1 Features

- AEC-Q100 Grade 2 Qualified
- Scalable Low Power Piezo Controller
  - Designed for TDK PowerHap 120 V Actuator Portfolio
  - Drives up to 4 µF
  - Energy Recovery
  - Small Solution Footprint
- Integrated Digital Front End with SPI
  - 1024-Samples Internal FIFO
  - 2-kB RAM Waveform Memory
  - Waveform Synthesizer
  - 1.8 V to 5.0 V Digital I/O Supply
- Piezo Sensing Interface
- Multi-Actuator Synchronization
- Fast Start-Up Time of 500 µs
- Connects to 12 V Power Bus
- Offered in a Wettable Flank QFN-24 Package

2 Applications

- Display Haptics
- Button Replacement
- Human Machine Interface

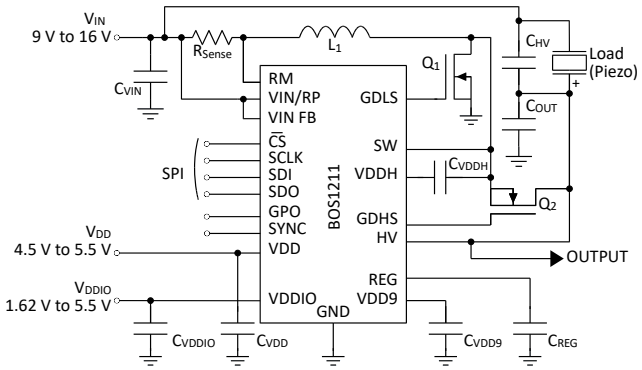


Figure 1: Simplified schematic

3 Description

The BOS1211 is a scalable piezo haptic controller based on our patented CapDrive™ technology. It can drive TDK's PowerHap 120 V piezo actuators or similar loads with up to 120 V HD haptic low distortion waveforms and operates from a 12 V supply voltage. The BOS1211 integrates a digital interface, low-side and high-side NMOS gate drivers for buck-boost conversion and piezo sensing capability.

The BOS1211 plays waveforms through its digital front-end and SPI interface. A flexible deep FIFO interface enables the user to continuously stream the digital waveform data for playback or to transmit burst data. The interface also integrates a waveform synthesizer and 2-kB RAM waveform memory to generate HD haptic waveforms with minimum communication bandwidth enabling two waveform generation modes: RAM playback and RAM synthesis.

The digital front-end gives access to many internal registers to optimize performance. The BOS1211 features a piezo sensing interface that can detect a pressure applied on the piezo actuator, play automatic haptic waveform feedback, and notify the host of the event.

The high-speed SPI enables the device to share a common communication bus for a multi-actuator system. The pin SYNC synchronizes multiple controllers in the same system to have waveforms phase delay within less than 2 µs.

Safety systems protect the device from damage in case of a fault.

Table 1: Product information

PART NUMBER	DESCRIPTION
BOS1211AQ	QFN 24L 4.0mm x 4.0mm

See section 10 for ordering information.

Table of Content

4 Pins Configuration and Functions

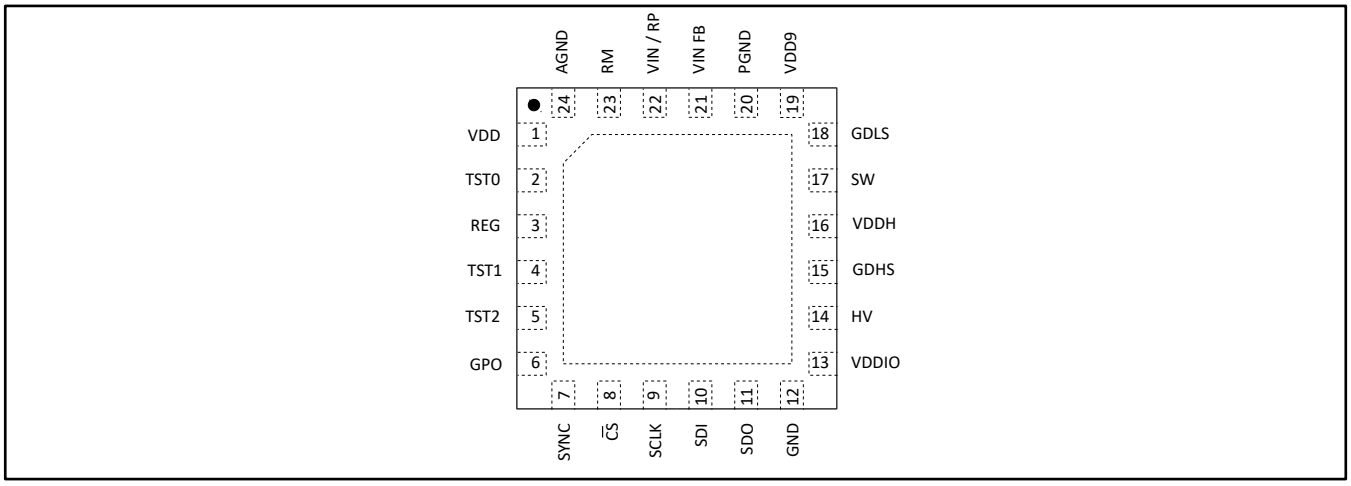


Figure 2: QFN 24L 4.0mm × 4.0 mm package with exposed thermal pad (TOP VIEW; NOT TO SCALE)

Table 2: QFN 24L 4.0mm x 4.0mm pin description

PIN NO.	PIN NAME	TYPE	DESCRIPTION
1	VDD	Power	Main controller supply
2	TST0	-	Factory test pin: must be kept floating
3	REG	Power	Internal 1.8 V regulator output
4	TST1	-	Factory test pin: must be kept floating
5	TST2	Input	Factory test pin: must be connected to GND
6	GPO	Output	Configurable output
7	SYNC	Input/Output	Multi-chip synchronizing pin
8	$\overline{CS}$	Input	SPI chip select
9	SCLK	Input	SPI clock
10	SDI	Input	SPI serial data in
11	SDO	Output	SPI serial data out
12	GND	Power	Power supply ground
13	VDDIO	Power	Power supply for digital IO
14	HV	Input	Voltage sense of high-voltage piezo signal
15	GDHS	Output	Gate driver output to high side NMOS switch
16	VDDH	Output	Floating supply for high side gate driver
17	SW	Input	Power converter switch pin
18	GDLS	Output	Gate driver output to low side NMOS switch
19	VDD9	Power	9 V internal gate driver supply
20	PGND	Power	Power supply ground connection to the low-side gate driver
21	VIN FB	Input	Voltage sense of low voltage piezo signal
22	VIN/RP	Power/Input	12 V Supply /Current sense positive input
23	RM	Input	Current sense negative input
24	AGND	Power	Power supply ground

5 Specifications

5.1 Absolute Maximum Ratings

Table 3: Absolute maximum ratings‡

	SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT
1		Voltage at pins HV, GDHS, GDLS, VDDH, SW	-0.3		140	V
2		Voltage at pins RM, VIN/RP, VIN FB	-0.3		28	V
3		Voltage at all other pins	-0.3		7	V
4	T_{stg}	Storage temperature	-65		150	°C
5	T_J	Junction temperature	-40		150	°C

‡Exceeding these values may cause permanent damage. Functional operation under these conditions is not guaranteed.

5.2 Package Thermal Information

Table 4: Package thermal information

	SYMBOL	PARAMETER	PACKAGE	MIN	NOM	MAX	UNIT
1	Θ_{JA}	Junction-to-ambient thermal resistance	QFN 24L 4.0mm x 4.0mm		28.8		°C/W

5.3 Recommended Operating Conditions

Table 5: Recommended operating conditions

	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
1	T_A	Operating Temperature	Operating free-air temp.	-40		105	°C
2	V_{IN}	Actuator input supply voltage		9		16	V
3	V_{DD}	Supply voltage		4.5		5.5	V
4	V_{DDIO} (1)	I/O Supply voltage		1.62		5.5	V
5	C_{ISS-Q2} (2)	Gate capacitance of Q_2				2	nf
6	C_{Load}	Load capacitance	f_{sig} = 300 Hz, V_{OUT} = 120 V			4	µF
7	L_1	Inductance			10		µH
8	R_{sense} (3)	Sense resistor		30		1000	mΩ
9	f_{OUT}	Output frequency		3.9		1000	Hz

(1) Digital I/O voltage (V_{DDIO}) must match with controller SPI interface voltage (MCU).
(2) C_{ISS-Q2} and C_{VDDH} determine the voltage at GDHS pin. See section 7.4.5 and 7.4.6 for more information.
(3) See section 7.4.3 for R_{sense} selection.

5.4 Electrical Characteristics

Table 6: Electrical characteristics. Conditions: T_A = -40°C to 105°C, V_{DD} = 5 V, V_{IN} = 12 V (unless otherwise noted)

	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
1	V_{REG}	Voltage at REG pin		1.75	1.80	1.85	V
2	V_{DD9}	Voltage at VDD9 pin			9.6		V
3	V_{IL}	Digital low-level input voltage (1)				0.5	V
4	V_{IH}	Digital high-level input voltage (1)		V_{DDIO}×0.7		V_{DDIO}+0.3	V
5	V_{OL}	Digital low-level output voltage (1)				0.4	V
6	V_{OH}	Digital high-level output voltage (1)		V_{DDIO}×0.8			
7	$V_{OUT(FS)}$	Full-scale OUTPUT voltage (at HV pin) (1)		117.5	120	122.5	V
8	I_{Q_VIN}	V_{IN} supply quiescent current	SLEEP IDLE, OE bit = 0x0 IDLE, OE bit = 0x1		6 14 350		µA
9	I_{Q_VDD}	V_{DD} supply quiescent current	SLEEP (1)		1	10	µA
			IDLE, OE bit = 0x0 IDLE, OE bit = 0x1		1 2	3.5 4	mA
10	$I_{VIN,AVG}$	Average V_{IN} supply current during operation	f_{sig} = DC (2) V_{OUT} = 120 V C_{Load} = 4 µF V_{IN} = 12 V		3		mA
			f_{sig} = 300 Hz V_{OUT} = 120 V C_{Load} = 4 µF V_{IN} = 12 V		250		mA
11	I_{GATELS}	Max. peak transient current at GDLS pin	Source, SLS= 0x3 Sink, SLS= 0x3		1200 850		mA
12	I_{GATEHS}	Max. peak transient current at GDHS pin	Source, SHS= 0x3 Sink, SHS= 0x3		1100 800		mA
13	V_{GATELS}	Voltage at GDLS pin activating Q_1			8.6		V
14	THD+N	Total Harmonic Distortion + Noise (1)	f_{sig} = 300 Hz V_{OUT} = 120 V C_{Load} = 4 µF			1	%
15	f_s	Sampling rate for waveform playback (3)	25°C, PLAY[2:0] = 0x0 25°C, PLAY[2:0] = 0x7	998 7.8	1024 8	1050 8.2	ksps
16	DHL	Sensing Detection to Haptic feedback latency (1)	Time from sensing detection event to automatic playback			100	µs

(1) Specification is assured by design and characterization data.
(2) PARCAP[7:0] bits can be adjusted to reduce power consumption for DC output.
(3) See Figure 12 for output frequency variation as a function of temperature.

5.5 Timing Characteristics (SPI)

Table 7: Timing characteristics. Conditions: T_A = -40°C to 105°C, V_{DDIO} = 3.3 V to 5.5 V, SDO load = 20 pF. Specifications are assured by design and characterization data.

	SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT
1	t_{clk}	Clock period (1)	28			ns
2	t_{clkL}	Clock Low period	15			ns
3	t_{clkH}	Clock High period	10			ns
4	t_L	Time between $\overline{CS}$ falling edge and SCLK rising edge	18			ns
5	t_H	Time between SCLK last falling edge and rising edge of $\overline{CS}$	15			ns
6	t_{CS}	$\overline{CS}$ High time between two transmissions (2)	150			ns
7	$t_{SDI,S}$	Input data setup time	4.5			ns
8	$t_{SDI,H}$	Input data hold time	3.5			ns
9	t_{SDO}	$\overline{CS}$ or SCLK falling edge to data output valid (1)			14	ns
10	t_{OZ}	$\overline{CS}$ rising edge to SDO high impedance			14	ns

(1) Specification depend on V_{DDIO} and SDO load, see Table 8.
(2) A minimum delay of 400 ns is required if the fist transaction is used to set BC[4:0] bits and the second transaction is used for data reading.

Table 8: Maximum SPI frequency vs. V_{DDIO} and SDO load.

	V_{DDIO}	MAXIMUM SPI FREQUENCY ($1/t_{clk}$)		UNIT
		SDO load = 20 pF	SDO load = 80 pF	
1	1.8 V	13	10	MHz
2	2.5 V	28	20	MHz
3	3.3 V	35	30	MHz
4	5.5 V	35	30	MHz

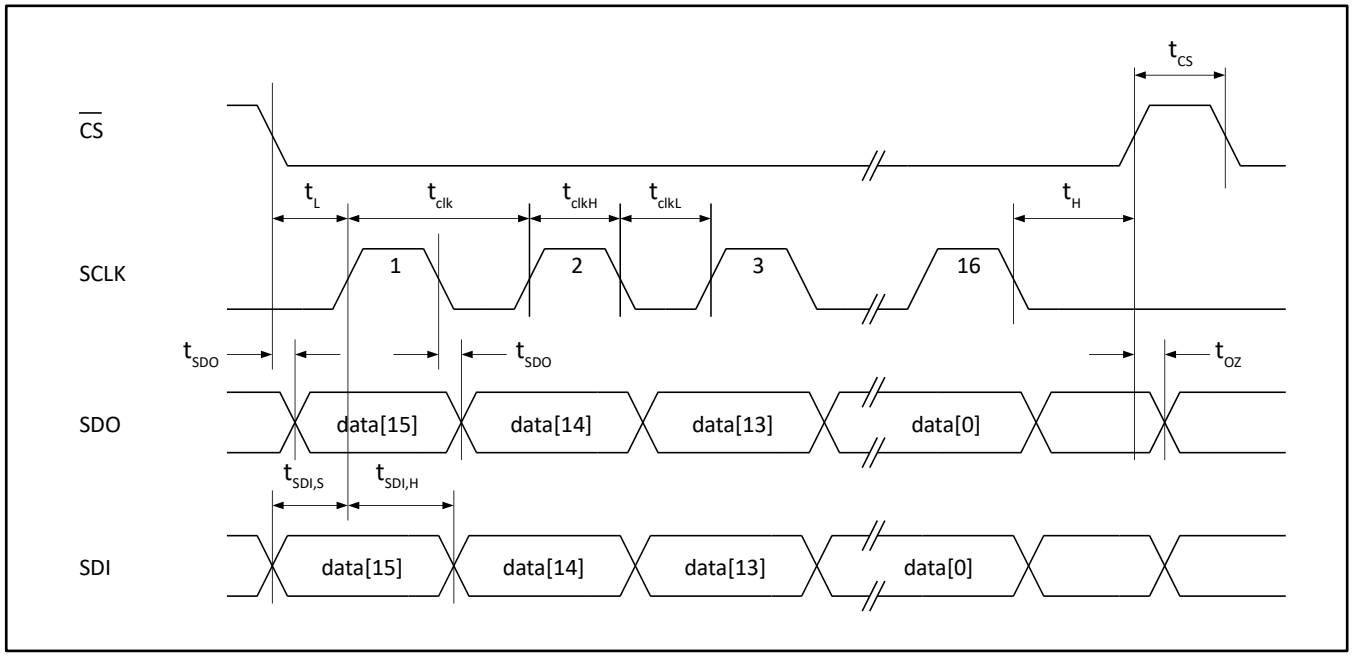


Figure 3: SPI timing diagram

5.6 Typical Performance Characteristics

Typical performance characteristics for the following conditions: T_A = 25°C, V_{IN} = 12 V, C_{OUT} = 4 µF, V_{OUT} = 120 V_{pk-pk} and f_{OUT} = 300 Hz (unless otherwise noted).

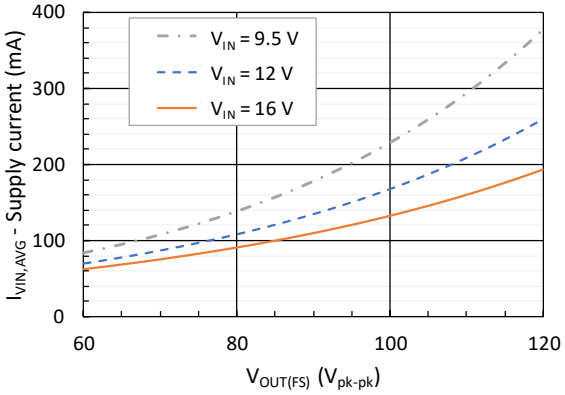


Figure 4: V_{IN} supply current vs output voltage

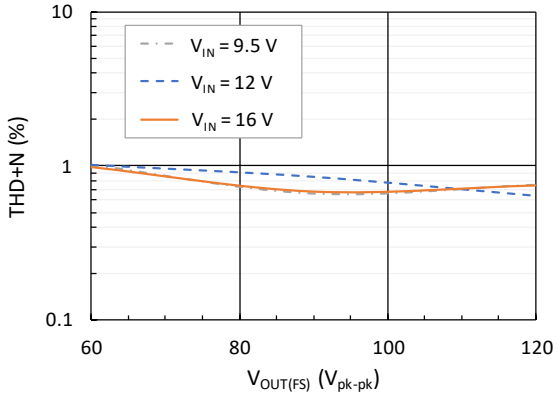


Figure 5: Total harmonic distortion + noise vs output voltage

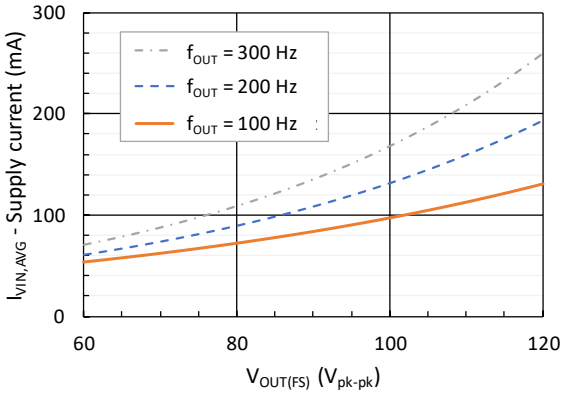


Figure 6: V_{IN} supply current vs output voltage

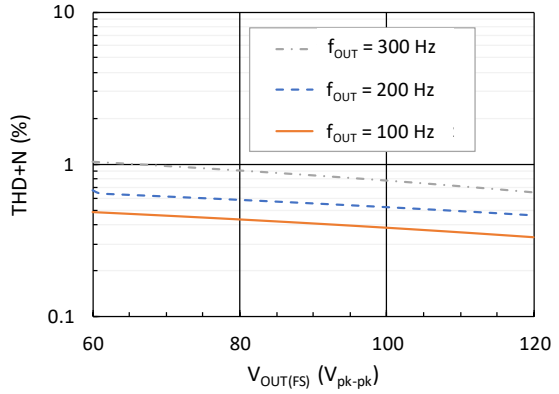


Figure 7: Total harmonic distortion + noise vs output voltage

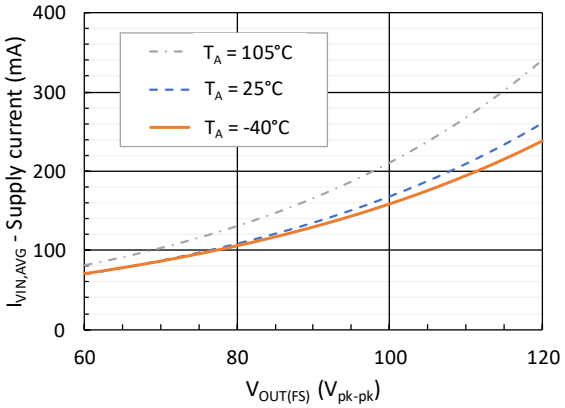


Figure 8: V_{IN} supply current vs operating free-air temperature

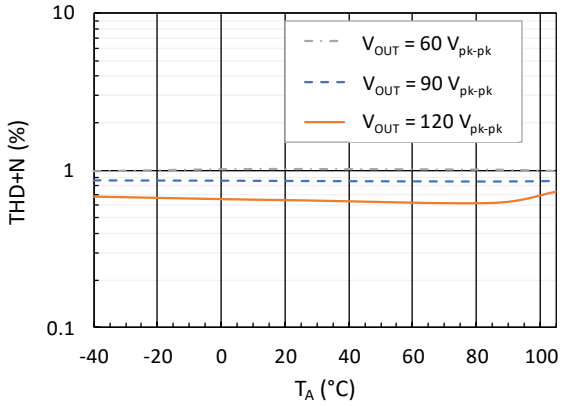


Figure 9: Total harmonic distortion + noise vs operating free-air temperature

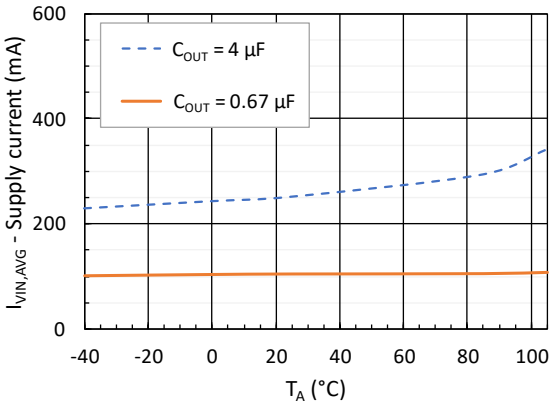


Figure 10: V_{IN} supply current vs operating free-air temperature

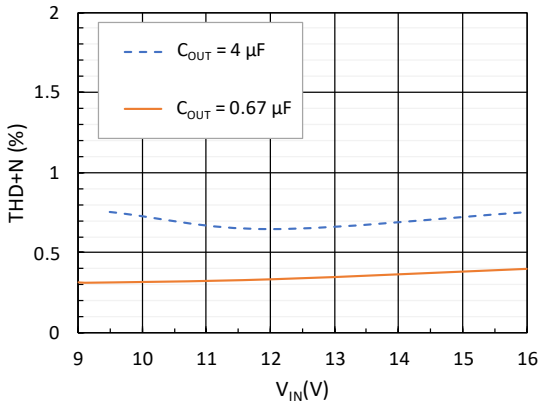


Figure 11: Total harmonic distortion + noise vs input voltage[2]

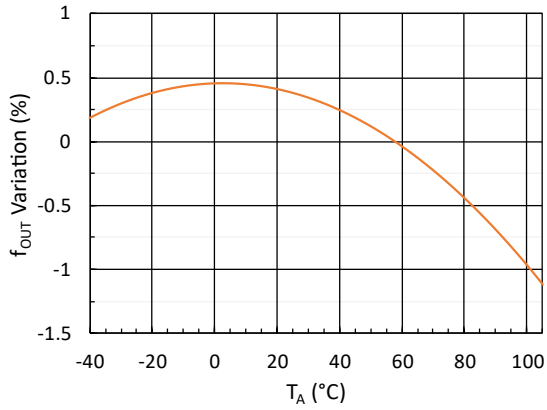


Figure 12: Output frequency variation vs operating free-air temperature

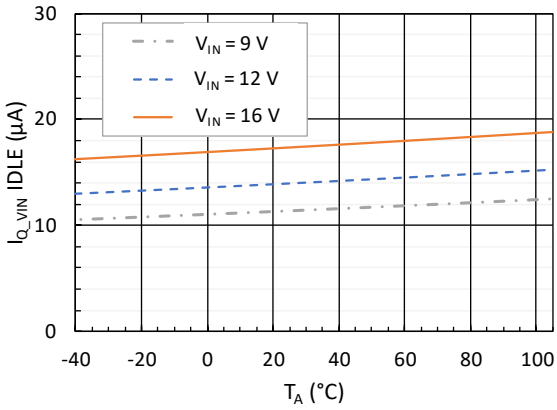


Figure 13: V_{IN} supply quiescent current in IDLE state vs operating free-air temperature

[2] Data for a load of 4 µF starts at a V_{IN} of 9.5 V because playing a waveform while having a V_{IN} lower than 9.5 V triggers the UVLO12 error flag.

6 Functional Description

6.1 Overview

The BOS1211 is a scalable haptic piezo actuator controller with integrated digital front end, including a FIFO and a Waveform Synthesizer (WFS). The BOS1211 implements a dynamic buck-boost conversion with energy recovery, based on Boreas's patented CapDrive™ Technology. The BOS1211 integrates a low-side and high-side NMOS gate drivers. The controller is compatible with 12 V systems. It can generate HD haptic waveforms with amplitude up to 120 V for a wide range of piezo actuators including TDK PowerHap 120 V portfolio. Interpolation between samples is done to smooth the haptic waveform.

The digital interface enables the user to stream the waveforms data from any MCU with an SPI port. A flexible FIFO interface enables the user to continuously stream the digital waveform data for playback or to transmit burst data. Data from the FIFO can be read at different sample rates. The digital front-end also integrates a Waveform Synthesizer (WFS) and 2-kB on-chip RAM with two waveform generation modes: RAM Playback and RAM Synthesis. These two modes allow haptic waveforms generation with minimal intervention from the host MCU.

The digital font-end gives access to many internal registers, enabling the user to optimize the performance of the device for a specific application. For instance, the voltage on the piezo actuator can be read at any time, allowing the development of advanced sensing algorithms and use a piezo actuator as a force sensor at the input of a system. Finally, the BOS1211 also includes an embedded sensing comparator enabling the controller to detect a pressure applied on a piezo actuator, automatically play a pre-programmed haptic waveform feedback and notify the MCU of an event.

The BOS1211 can use many commercial off-the-shelf (COTS) inductors. The inductor can be chosen to optimize the power, size or performance trade-off for the user application. With a start-up time of less than 500 µs from SLEEP state, the BOS1211 is ideal for low latency haptic feedback.

6.2 Features

6.2.1 Digital Front-End Interface

The BOS1211 uses a 35 MHz SPI target interface. This high-speed communication interface enables to share a common communication bus for multi-actuator systems. The digital front-end gives access to internal registers that control the device operation and performance, see section 7.5 for details.

6.2.2 GPO

One general-purpose digital output (GPO) is available and can be used as an interruption to notify the host MCU of various events using GPO[2:0] bits such as haptic detection events or an error. The GPO is a push-pull output between V_{DDIO} and GND.

6.2.3 Flexible Haptic Waveform Generation

6.2.3.1 Direct Mode

With MODE[1:0] bits set to 0x0, the haptic waveform samples are played as they are sent from the host MCU to RAM using REFERENCE register. The rate at which the RAM data is read to generate the haptic waveform is set by PLAY[2:0] bits. See section 6.5 for details.

6.2.3.2 FIFO Mode

A 1024-sample FIFO is available for waveform playback with MODE[1:0] bits set to 0x1. The FIFO entries are appended every time waveform samples are written in the REFERENCE register. Digital samples are represented as 12-bit unsigned values. If OE bit is set to 0x1, the FIFO entries are read automatically out of the FIFO at a rate set by PLAY[2:0] bits. See section 6.6 for more details.

6.2.3.3 RAM Playback Mode

RAM Playback mode is selected with MODE[1:0] bits set to 0x2. In RAM Playback mode, the on-chip RAM of 2 kB is used to store haptic waveforms as waveform amplitude samples in 12-bit unsigned format with minimum interventions from the MCU. The waveform is sampled at a rate set by PLAY[2:0] bits. See section 6.7 for details.

6.2.3.4 RAM Synthesis Mode

RAM Synthesis mode is selected with MODE[1:0] bits set to 0x3. In RAM Synthesis mode, the BOS1211 uses the Waveform Synthesizer (WFS) to generate waveforms using parameters stored in the 2 kB RAM. RAM Synthesis mode allows generating sinusoidal waveforms of various amplitudes and frequencies without having to send every sample of the waveform to RAM as is the case with RAM Playback mode. This allows complex waveforms to be produced with minimal data communication. See section 6.8 for details.

6.2.4 SLEEP state

When no haptic waveform is being requested (OE bit set to 0x0), the BOS1211 can enter in one of the two low-power modes: IDLE or SLEEP state. DS bit sets the device power mode when no haptic waveform is requested. By default, the power mode is IDLE (DS bit set to 0x0). SLEEP state is selected when DS bit is set to 0x1. In SLEEP, the BOS1211 is in its lowest power state and all registers are set back to their default values as well as the RAM data is reset. The BOS1211 goes out of SLEEP state on pin $\overline{CS}$ falling edge.

6.2.5 Low Latency Startup

The BOS1211 features a fast start-up time. From IDLE or SLEEP state, the device takes approximately 500 µs to start playing the waveform when the auto-calibration piezo zeroing is set to 500 µs (SHORT[1:0] bits set to 0x0).That makes the BOS1211 a very small contributor to system latency.

6.2.6 Piezo Actuator Sensing

The digital front-end gives access to internal registers 0xA and 0x12 that allow the use of piezo actuators as a force sensor.

The BOS1211 features an embedded sensing comparator that can be configured to detect a sensing event. The sensing comparator can adapt to a specific application by setting its voltage threshold (STHRESH[8:0] bits), hold time (REP[2:0]) and crossing direction (SIGN bit).

It is also possible to automatically trigger an programmed waveform when a sensing event is detected by the sensing comparator. GPO output pin can be configured using GPO[2:0] bits to inform the MCU that a sensing event occurred or that the triggered waveform has finished playing. Setting BC[4:0] bits to 0x12 will output sensing voltage data, which can be read at any time and is useful for MCU-based customized sensing algorithms. See section 6.9 for details.

6.2.7 Device Reset

The BOS1211 device has software-based reset functionality. When RST bit is set, all registers are set to their default value and the BOS1211 goes to IDLE state. RST bit self-clears once the reset is complete.

The following sequence must be done to safely reset the device while playing a waveform in FIFO or Direct mode:

1. Set CONFIG.OE bit must be set to 0x0.
2. Wait for the device to be in IDLE by polling IC_STATUS.STATE[1:0] bits.
3. Reset the device by setting RST bit to 0x1.

6.2.8 Actuator Synchronization

Multiple BOS1211 devices can play haptic waveforms simultaneously using the SYNC pin. This feature allows synchronizing a waveform across several devices with a phase delay of less than 2 µs between them.

Synchronization is achieved by connecting the SYNC pin of all devices together. A 10 kΩ pull-up resistor is needed between SYNC pin node and V_{DDIO}. Synchronization is performed as the wave is played with a signal on the SYNC pin having a frequency that depends on the sampling rate defined by PLAY[2:0] bits.

The following sequence presents an example allowing synchronizing two BOS1211 devices:

1. On both devices perform the following configuration:
    a. In the CONFIG register:
        i. Set CONFIG.OE bit to 0x0 to disable the haptic waveform generation.
        ii. Set CONFIG.PLAY[2:0] bits to the desired sampling rate.
        iii. Set CONFIG.SYNC bit to 0x1 to enable device synchronization.
    b. Set RAM.MODE[1:0] bits to 0x2 or 0x3 to select RAM Playback or RAM Synthesis mode.
    c. Properly configure the waveform depending on the mode selected (see section 6.7 or 6.8).
2. Set CONFIG.OE bit to 0x1 on device 1.
3. Set CONFIG.OE bit to 0x1 on device 2 and waveform will start playing on both devices.

6.2.9 Adjustable Current Limit

The maximum current of the BOS1211 power converter must be limited to avoid damage to the inductor. Current flowing in the inductor is determined by the BOS1211 by measuring the voltage drop across R_{sense} placed between pins VIN/RP and RM. The current limit of the power converter is adjusted by selecting the proper R_{sense} value (see section 7.4.3 for more detail).

The current limit of Q_1 and Q_2 NMOS transistors should be selected based on the following:

- Ensure that the current is lower than the saturation limit of the inductor L_1.
- Ensure that the current is high enough to allow sufficient energy transfer to and from the piezo actuator.

The circuit should be tested under worst-case conditions to ensure that the BOS1211 will meet the bandwidth requirement of the application (see section 7.4.5 for more detail).

6.2.10 Energy Recovery

The BOS1211 implements bidirectional power transfer: input (V_{IN}) to OUTPUT, and OUTPUT to input (V_{IN}), which makes the device power efficient. Such architecture enables the recovery of the energy accumulated on the capacitive load and transfers it back to the input (C_{VIN}). The internal controller determines the direction of the power flow during waveform playback.

6.2.11 Adjustable Internal Clock

The internal BOS1211 clock oscillator frequency is trimmed during fabrication using hardware fuses. When initialized, the BOS1211 retrieves the hardware fuse values and push them to the TRIM block to adjust the oscillator frequency based on the fuse values (Figure 21). The TRIM register allows modifying the TRIM value to adjust oscillator frequency.

This feature can be used to match the external system clock frequency with the BOS1211 internal clock frequency, which is used to determine the FIFO read-out rate. This might be needed to minimize waveforms distortion if the user writes waveform data at a constant rate to the FIFO, without managing space available in it. To successfully adjust internal clock frequency, OE bit must be set to 0x0.

The internal oscillator can be adjusted with the following sequence:

1. Set OE bit to 0x0.
2. Set TRIM.TRIMRW[1:0] bits to either one of the following values:
    a. Set to 0x1 to latch the hardware fuses and push their value into the TRIM block and the TRIM register, or
    b. Set to 0x2 to retrieve the oscillator trim value contained in the TRIM block and push it to the TRIM register.
3. Wait for 1 ms.
4. Read TRIM.TRIM_OSC[6:0] bits to get the internal oscillator trim value specific to the device.
5. In one transaction, set the TRIM register with the following fields:
    a. TRIM.TRIM_OSC[6:0] bits set to the desired value.
    b. TRIM.TRIMRW[1:0] bits set to 0x3 to write TRIM_OSC[6:0] value to TRIM block.

The same procedure can be used to adjust the internal 1.8 V regulator voltage using TRIM_REG[2:0] bit instead of TRIM_OSC[6:0].

6.2.12 Fault Behavior

This section lists the various faults detected by the device. Note that the faults detected by the device may be caused by the following:

- Device operating outside of its safe operating conditions.
- Wrong component value (e.g., R_{sense}, C_{HV} or L_1).
- Noise induced by improper printed circuit board layout.

If one of the following faults is detected, the device will safely ramp down the OUTPUT node voltage to V_{IN} and raise an error flag with a specific error code.

6.2.12.1 Overvoltage

If an overvoltage condition at the HV pin is detected during waveform generation, OVV bit is set, and the OUTPUT node voltage will safely ramp down to V_{DD}. A software reset (RST bit set to 0x1) is required to clear the fault and resume normal operation.

6.2.12.2 Output Short Circuit

The BOS1211 has an output short circuit protection to prevent excessive current to flow because of a short-circuit load. In case the short circuit condition is detected during waveform generation, SC bit is set and BOS1211 is put in IDLE state. A software reset (RST bit set to 0x1) is required to clear the fault and resume normal operation.

6.2.12.3 Overtemperature

The BOS1211 has an internal temperature sensor that puts the device in IDLE state in case the die temperature exceeds 145 °C. In this condition, OVT bit is set and will clear automatically once conditions are safe for a restart.

The BOS1211 device is unlikely to reach 145 °C even during continuous operation at maximum load in the T_A operating range because of its low power dissipation.

6.2.12.4 Brownout

The BOS1211 has internal brownout protections. If V_{REG} goes below 1 V, the device issues a reset signal, and all registers are set back to their default value. When V_{REG} goes back to a normal operating voltage, the BOS1211 goes to the IDLE state.

6.2.12.5 Under Voltage/Over Voltage Lockout

The controller also monitors the V_{IN} and V_{DD} supplies to ensure the minimum conditions are met to operate. The controller won't start a waveform if the voltage is below or above specified limits. Table 9 presents those limits.

If an under/overvoltage condition at V_{IN} is detected during waveform generation, the following events occur:

- UVLO12/OVLO12 bit is set to 0x1.
- STATE[1:0] bits are set to 0x3 (ERROR state).

If an undervoltage condition at V_{DD} is detected, the following events occur:

- UVLO5 bit is set to 0x1.
- STATE[1:0] bits are set to 0x3 (ERROR state).

The BOS1211 will go to IDLE state (STATE[1:0] bits to 0x0) with the following conditions:

- V_{IN} and V_{DD} go back to a normal operating voltage.
- OE bit is reset to 0x0.

Table 9: Under voltage / over voltage lockout limits

Supply	UVLO limit	OVLO limit	Unit
V_{IN}	8.8	19.9	V
V_{DD}	4.4	N/A	V

6.2.12.6 Current Detection Status Fault

For proper operation, the BOS1211 monitors the current using R_{sense} resistor connected to VIN/RP and RM pins. If no current is detected during waveform generation, the following event occurs:

- IC_STATUS.IDAC fault bit is set.
- IC_STATUS.STATE[1:0] bits are changed to 0x3 (ERROR state).

Typically, IDAC bit is set when R_{sense} or L_1 is disconnected.

The BOS1211 will go to IDLE state (STATE[10] bits to 0x0) with the following conditions:

- V_{IN} and V_{DD} go back to a normal operating voltage.
- OE bit is reset to 0x0.

6.3 Automatic Output Shutdown

TOUT bit allows programming a 4 ms timeout delay after which the device will automatically go to SLEEP if it didn't receive a proper communication on its digital interface.

6.4 SPI Interface

A target SPI port enables communication with the BOS1211. SPI is a 4-wire synchronous serial interface that uses two control lines and two data lines: Chip Select ($\overline{CS}$), Serial Clock (SCLK), Serial Data Output (SDO) and Serial Data Input (SDI). These signals are in the V_{DDIO} voltage domain.

The SPI interface supports 16 bits per transfer. Transfer is done in full duplex: data is output on SDO at the same time data is sent on SDI.

SPI transmission starts when $\overline{CS}$ line goes low and ends when $\overline{CS}$ line goes high. Each SPI target device requires its own $\overline{CS}$ line from the controller. The Figure 14 shows the correct configuration for the SPI Controller. Because different manufacturers have different definitions of SPI modes, the user should rely on Figure 14 to select the appropriate SPI mode for its MCU.

The SPI communication bus features the following:

1. Each transmission is 16 bits.
2. MSB is sent first.
3. Data is latched on the rising edge of SCLK.
4. Input Data should be transitioned on the falling edge of SCLK.
5. Data rates up to 35 Mbps are supported.
6. Single and burst read/write transmissions are supported. For burst data transmission, $\overline{CS}$ line can be maintained low.

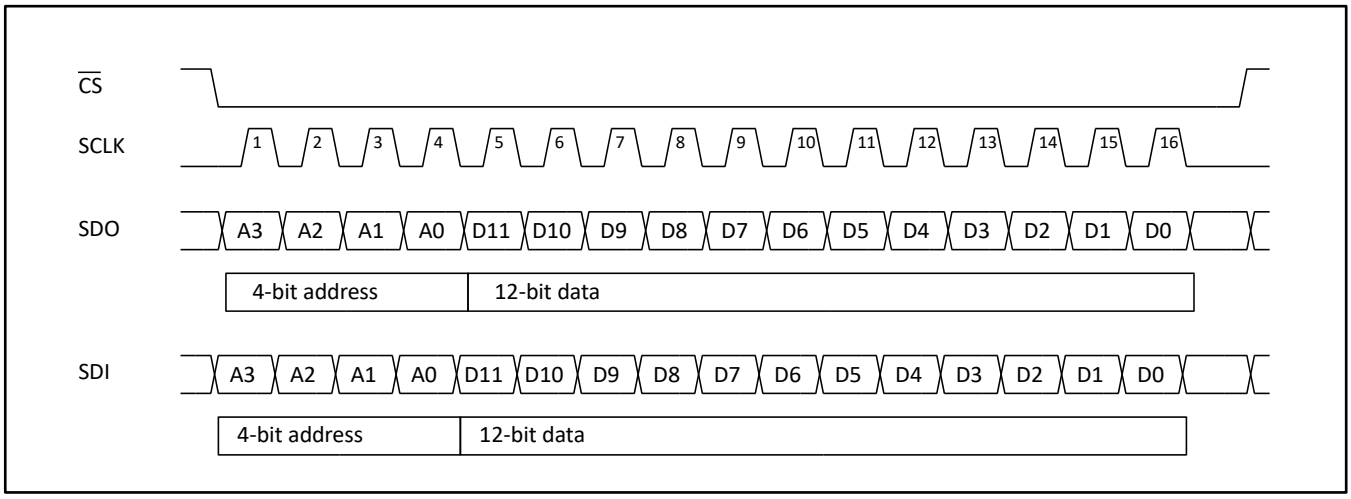


Figure 14: SPI typical specification

6.5 Direct Mode

In Direct mode (MODE[1:0] bits set to 0x0), the haptic waveform samples are played as they are sent from the host MCU to the REFERENCE register. The rate at which the data is read to generate the haptic waveform is set by PLAY[2:0] bits.

Data management and synchronization can be facilitated by setting GPO [2:0] bits to 0x7 to allow the GPO to generate an interruption pulse that notifies the MCU when the device is ready to receive the next sample.

When MODE[1:0] bits is set to 0x0 to use Direct mode, RAM is not used and its content previously written using RAM Playback mode (section 6.7) or RAM Synthesis mode (section 6.8) is preserved.

Note that waveforms should begin and end with 0 V amplitude.

6.5.1 Typical Operation Sequence

The following sequence use Direct mode to play haptic waveforms:

1. Set RAM.MODE[1:0] bits to 0x0 to select Direct mode.
2. In the CONFIG register:
    a. Set CONFIG.OE to 0x1.
    b. Set CONFIG.PLAY[2:0] to the desired sampling rate.
3. Set SPI.GPO[2:0] bits to 0x7 to allow the GPO pin to generate an interruption to notify the MCU when the device is ready to receive the next sample.
4. Write the 12-bit waveform data into the REFERENCE register.
5. Monitor the GPO pin and wait until the device is ready to receive the next sample.
6. Repeat step 4 and 5 until the desired waveform is completed.

6.6 FIFO Mode

In FIFO mode (MODE[1:0] bits set to 0x1), the waveform playback is set in a 1024-sample FIFO. The FIFO entries are appended every time waveform data is written in the REFERENCE register. Digital samples are represented as 12-bit unsigned values. The waveform is played when OE bit is set to 0x1 at a rate set by PLAY [2:0] bits. For waveform playback streaming, the user should ensure the FIFO never becomes empty. If the FIFO becomes empty, EMPTY bit is set and the FIFO maintains the last valid data, keeping the waveform in a steady state. FULL bit is set when the FIFO is full and cannot accept more data.

Burst data transfers can be used to minimize the communication interface usage (see section 6.4). In this use case, packets of 16-bit words can sequentially be written in the FIFO at a maximum speed of 35 Mbps. FIFO_SPACE [9:0] field can be read prior writing burst data to validate the space available.

Waveforms should begin and end with 0 V amplitude. If OE bit is set to 0x0 during waveform playback, the voltage across the piezo actuator will be ramped down to 0 V and the remaining data in the FIFO will be preserved.

The device uses RAM to implement FIFO. Using FIFO mode overwrites any waveform data previously programmed using RAM Playback mode (section 6.7) or RAM Synthesis mode (section 6.8).

Note the following:

- For waveform playback streaming, the FIFO data write rate must match the readout rate of the waveform playback set by PLAY[2:0] bits to always keep valid data inside the FIFO. The EMPTY bit is set to 0x1 when the FIFO becomes empty, causing the FIFO to hold the last valid data and keep the output waveform in a steady state.
- Waveforms should begin and end with 0 V amplitude.
- In case OE bit is set to 0x0 during waveform playback, the output will ramp down automatically to 0 V and the remaining FIFO entries will be kept and played the next time OE bit is set to 0x1 again.

6.6.1 Typical Operation Sequence

The following sequence use FIFO mode to play haptic waveforms:

1. Set RAM.MODE[1:0] bits to 0x1 to select FIFO mode.
2. In the CONFIG register:
    a. Set CONFIG.OE bit to 0x1 to enable the haptic waveform generation.
    b. Set CONFIG.PLAY[2:0] bits to the desired sampling rate.
3. Read FIFO_STATUS register to determine how much space is available in the FIFO for new data.
4. Write as much 12-bit waveform data as possible according to the available space in the FIFO into the REFERENCE register.
5. Read FULL bit to determine if the FIFO can accept more data.
    a. If more data can be accepted, repeat steps 3, 4 and 5 until the desired waveform is completed.
    b. If the FIFO is FULL repeat step 5.

6.6.2 FIFO Example

In section 6.6.1, the FIFO is filled after setting OE bit to 0x1. Table 10 is an example where the waveform data is written in the FIFO before setting OE bit to 0x1.

Table 10: FIFO mode example

Code	Description
Configure for FIFO mode:	
0x8001	Select FIFO mode to RAM register.
Write Data to FIFO:	
0x0000	Write waveform sample data to REFERENCE register.
0x0066	
0x00CC	
0x0132	
0x0198	
0x01FE	
0x0264	
0x02CA	
0x0330	
0x0393	
0x0330	
0x02CA	
0x0264	
0x01FE	
0x0198	
0x0132	
0x00CC	
0x0066	
0x0000	
Configure the Waveform Start:	
0x5017	Set CONFIG.OE bit to 0x1 to start haptic waveform playback.

6.7 RAM Playback

In RAM Playback mode (MODE bits set to 0x2), the waveform to be played is defined by storing all the amplitude samples in sequence in RAM. The waveform is played when OE bit is set to 0x1.

The samples are written to RAM using the BURST RAM WRITE WFS command. More than one waveform can be stored in RAM. The 2 kB memory can store up to 1024 samples. Each sample defines a 16-bit data word containing the 12-bit waveform amplitude in the 12 LSBs of that word and using the same format as the REFERENCE register. The start and end RAM address must be stored in the RAM PLAYBACK command, which indicates the RAM address of the samples to be fetched when the playback is initiated.

When playback starts, the data is read out sequentially at the sample rate set by PLAY [2:0] bits. An interpolation is done between user samples to generate the output waveform when PLAY [2:0] bits are 0x1 to 0x7.

The start and end RAM addresses must be written again using the RAM PLAYBACK command each time a waveform already programmed in RAM needs to be played again (see section 6.7.1).

Note that waveforms should begin and end with 0 V amplitude.

6.7.1 Typical Operation Sequence

The following sequence shows how to use RAM Playback mode to play haptic waveforms:

1. In the RAM register:
    a. Set RAM.MODE[1:0] to 0x2 to select RAM playback mode.
    b. Set RAM.RAMSEL to 0x1 so that subsequent SPI communication is sent to the WFS command interpreter.
2. Program RAM using BURST RAM WRITE command. See section 6.7.2 for an example. To keep access to the WFS command interpreter, make sure the SPI transactions are sent within 4 µs of each other to continue writing in RAM.
3. Write the start and end RAM address using RAM PLAYBACK WFS command.
4. Wait for more than 4 µs to access to the main register map.
5. Set BC[4:0] to 0xC to output IC_STATUS register content on SDO pin.
6. In the CONFIG register:
    a. Set CONFIG.OE bit to 0x1 to start haptic waveform playback.
    b. Set CONFIG.PLAY[2:0] bits to the desired sampling rate.
7. Poll EMPTY bit on SDO communication port until it is set to 0x1 and waveform is completed.
8. Set CONFIG.OE bit to 0x0 to deactivate haptic waveform playback.

To start playback with sensing detection, the sensing parameters can be configured between step 4. and 5. See section 6.9 for sensing configuration details.

6.7.2 RAM Playback Example

An example of waveform playback is presented in Table 11 where a waveform of 9 samples is played. Table 12 is an example where a waveform already programmed in RAM is played.

Table 11: Example of playing a haptic waveform using RAM Playback mode

Code	Description
Configure RAM playback:	
0x8006	Select RAM Playback mode and request access to the WFS command interpreter. The following SPI transactions must be sent less than 4 µs from each other to keep using WFS command interpreter.
0x0014	Use BURST RAM WRITE WFS command.
0x0000	Set RAM start RAM address to 0x0000.
0x000A	Set Data count (10 samples to be written starting at address 0x0000).
0x0000	Sample Data at RAM address 0x0000.
0x0066	Sample Data at RAM address 0x0001.
0x00CC	Sample Data at RAM address 0x0002.
0x0132	Sample Data at RAM address 0x0003.
0x0198	Sample Data at RAM address 0x0004.
0x0198	Sample Data at RAM address 0x0005.
0x0132	Sample Data at RAM address 0x0006.
0x00CC	Sample Data at RAM address 0x0007.
0x0066	Sample Data at RAM address 0x0008.
0x0000	Sample Data at RAM address 0x0009.
0x0013	Use RAM Playback WFS command.
0x0000	Set RAM Playback start address to 0x0000.
0x0009	Set RAM Playback end address to 0x0008.
Wait for more than 4 µs to access to the main registers.	
Start and stop waveform playback:	
0x9628	Set BC[4:0] to 0xC to output IC_STATUS register content on SDO pin.
0x5017	Set OE bit to 0x1 to start haptic waveform playback.
0x0000	Poll EMPTY bit on SDO communication port until it is set to 0x1 and waveform is completed.
0x5007	Set OE bit to 0x0 to deactivate haptic waveform playback.

Table 12: Example of playing a haptic waveform already programmed in RAM using RAM Playback mode

Code	Description
Set start and end RAM addresses:	
0x8006	Select RAM Playback mode and request access to the WFS command interpreter. The following SPI transactions must be sent less than 4 µs from each other to keep using WFS command interpreter.
0x0013	Use RAM Playback WFS command.
0x0000	Set RAM Playback start address to 0x0000.
0x0009	Set RAM Playback end address to 0x0008.
Wait for more than 4 µs to access to the main registers.	
Start and stop waveform playback:	
0x9628	Set BC[4:0] to 0xC to output IC_STATUS register content on SDO pin.
0x5017	Set OE bit to 0x1 to start haptic waveform playback and PLAY[2:0] to set sample rate to 8 ksps.
0x0000	Poll EMPTY bit on SDO communication port until it is set to 0x1 and waveform is completed.
0x5007	Set OE bit to 0x0 to deactivate haptic waveform playback.

6.8 RAM Synthesis Mode

In RAM Synthesis mode (MODE bits set to 0x3), RAM stores sine wave parameters to generate simple and complex waveforms using the following:

1) SLICEs, written in RAM using the RAM SYNTHESIS WRITE command. Each SLICE contains a group of parameters used to produce a sine wave of defined amplitude, frequency, and number of cycles. It may also be ramped up and down (as shown in Figure 17). See section 6.8.1.1 for more details.
2) WAVEs, written in RAM using the RAM SYNTHESIS WRITE WFS command. A WAVE defines a series of SLICEs to be played successively. All SLICEs of a WAVE must be written in order and contiguously in RAM. See section 6.8.1.2. for more details.
3) SEQUENCEs, written using the SEQUENCER WFS command. The SEQUENCER command is used to store up to 15 WAVE addresses in RAM (called WAVEFORM_IDs). The WAVEs may all be played sequentially, or in any contiguous subsets, down to a single WAVEFORM_ID. See section 6.8.1.3 for more details.

The SEQUENCE_START/STOP WFS command defines the start and end WAVEFORM_IDs from the WAVEFORM_IDs list stored using the SEQUENCER command.

The start and end WAVEFORM_IDs must be written again using the SEQUENCE_START/STOP WFS command each time a waveform already programmed in RAM needs to be played again (see section 6.8.3).

6.8.1 RAM Programming

WAVE and SLICE data are stored in RAM. RAM is divided in two sections as shown in Figure 15. The first section stores the WAVE blocks, and the second section stores the SLICEs.

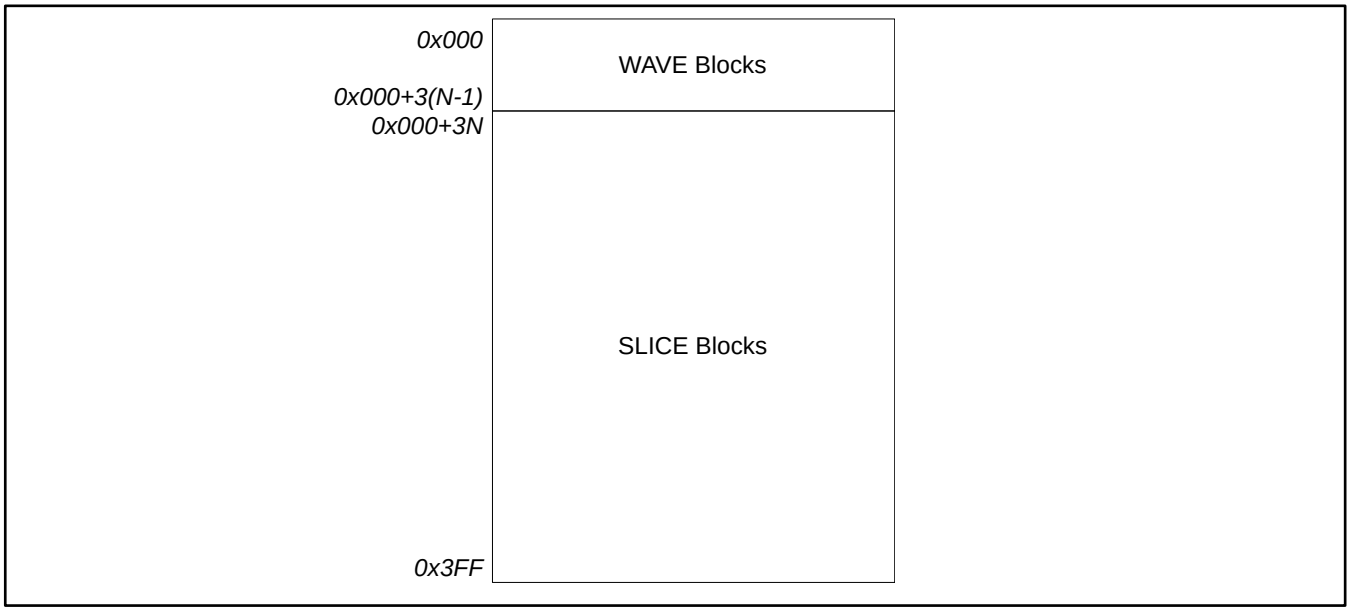


Figure 15: Example of N WAVE blocks followed with SLICEs organized in RAM (1024 × 16-Bit)

6.8.1.1 SLICE Blocks

SLICE blocks in RAM contains the parameters used to synthesize sine waveforms. Each SLICE block contains three words grouping five parameters as described in Figure 16 and Table 13. The Figure 17 illustrates how SLICE parameters shape a SLICE waveform. Many SLICEs may be successively played to form complex waveforms.

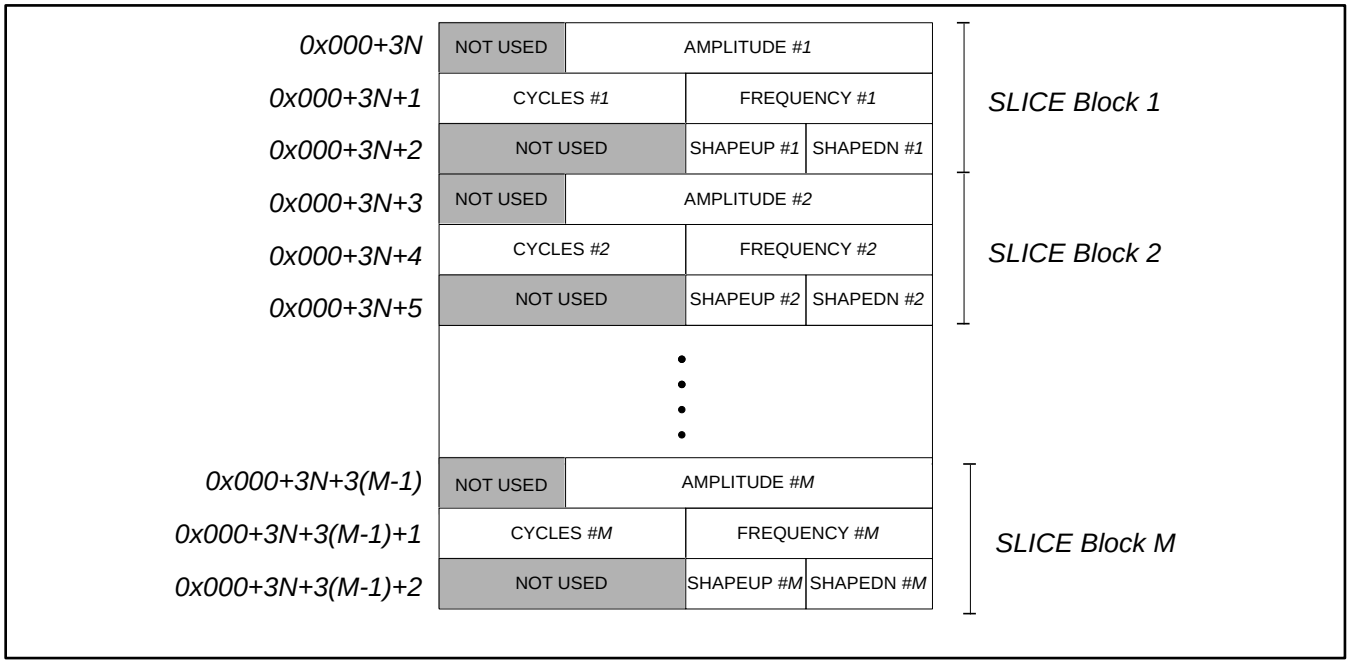


Figure 16: M SLICE blocks in RAM preceded by N WAVE blocs

Table 13: Sine wave SLICE parameters

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOT USED: 0x0				AMPLITUDE[11:0]											
CYCLES[7:0]								FREQUENCY[7:0]							
NOT USED: 0x00								SHAPEUP[3:0]				SHAPEDN[3:0]			

WORD	BITS	NAME	DESCRIPTION
1	11:0	AMPLITUDE	Sets the output waveform peak voltage amplitude (V_{OUT-pk}) as follows: $$AMPLITUDE[11:0] = \frac{4095 \times V_{OUT-pk}}{120}$$ This AMPLITUDE value calculation is valid only for RAM Synthesis mode (MODE[1:0] bits set to 0x3).
2	15:8	CYCLES	CYCLES refers to the number of times a full sine wave period will be repeated, excluding the ramp-up and ramp-down duration set by SHAPEUP[3:0] and SHAPEDN[3:0].
2	7:0	FREQUENCY	The waveform synthesizer has a frequency resolution of 3.9 Hz. The synthesized sine wave frequency will be: $$\text{Synthesized sine wave frequency (Hz)} = 3.9 \times FREQUENCY$$
3	7:4	SHAPEUP	SHAPEUP [3:0] sets the time to ramp up from 0 V to V_{OUT-PK}. SHAPEDN[3:0] sets the time required to ramp down from V_{OUT-pk} to 0 V. SHAPEUP and SHAPEDN duration must be greater than the waveform period and are added to the SLICE waveform duration. The SLICE waveform duration in *ms* (t_{SLICE}) is calculated as follows: $$t_{SLICE} = SHAPEUP + \frac{CYCLES[7:0]}{3.9 \times FREQUENCY} + SHAPEDN$$ 0x0: No shape 0x1: 32 ms 0x2: 64 ms 0x3: 96 ms 0x4: 128 ms 0x5: 160 ms 0x6: 192 ms 0x7: 224 ms 0x8: 256 ms 0x9: 512 ms 0xA: 768 ms 0xB: 1024 ms 0xC: 1280 ms 0xD: 1536 ms 0xE: 1792 ms 0xF: 2048 ms
3	3:0	SHAPEDN	

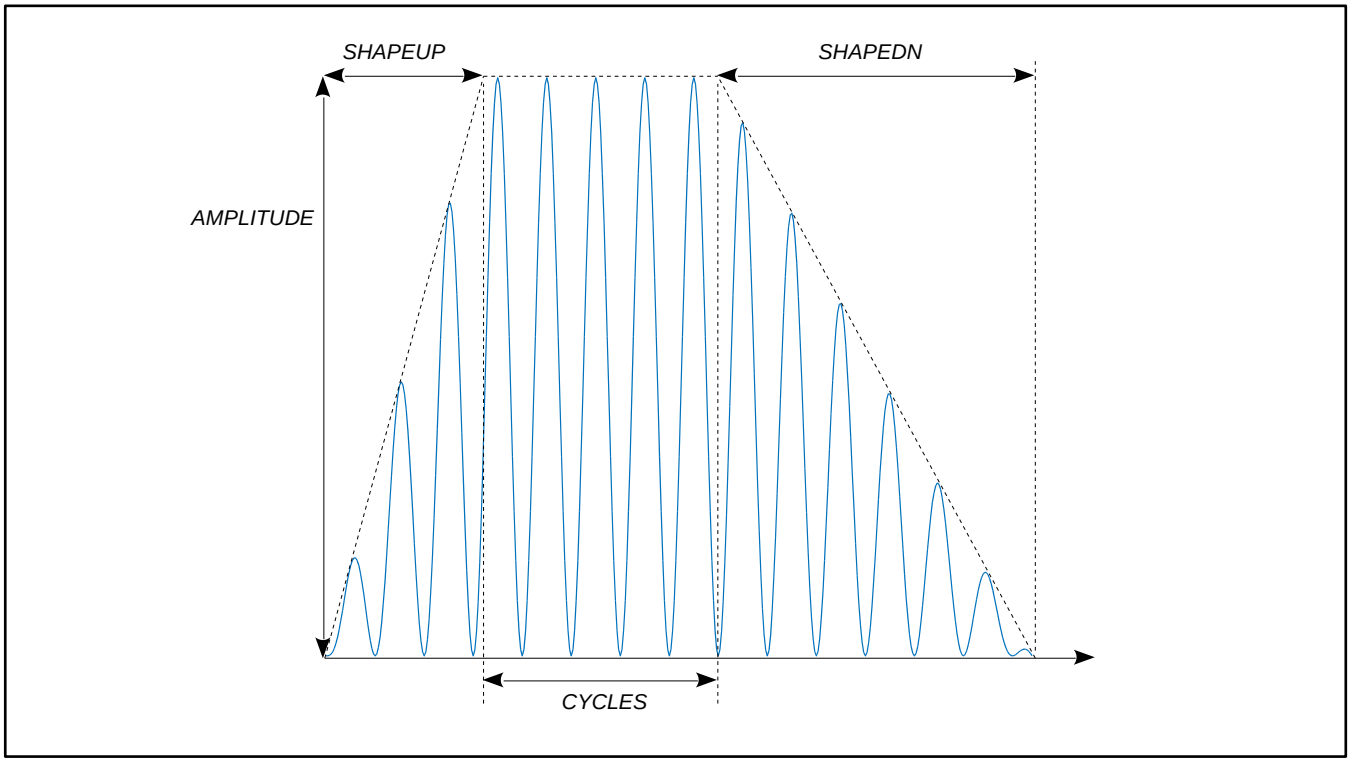


Figure 17: Sine wave SLICE parameters illustration

6.8.1.2 WAVE Blocks

As shown in Table 14 and Figure 18, each WAVE block in RAM contains three words:

1. The SLICE START ADDRESS [9:0]
2. The SLICE END ADDRESS [9:0]
3. The WAVE CYCLE COUNT [15:0]

SLICEs to be played sequentially must be placed contiguously in RAM.

Table 14: Wave block description

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NOT USED: 0x00						SLICE START ADDRESS[9:0]									
NOT USED: 0x00						SLICE END ADDRESS[9:0]									
WAVE CYCLE COUNT[15:0]															

WORD	BITS	NAME	DESCRIPTION
1	9:0	SLICE START ADDRESS	Defines RAM address of the first SLICE block (location of its first word).
2	9:0	SLICE END ADDRESS	Defines RAM address of the last SLICE block (location of its last word).
3	15:0	WAVE CYCLE COUNT	Sets the number of times the WAVE block is repeated. If the CYCLE COUNT is set to zero, it will be considered as a request to play the WAVE only once.

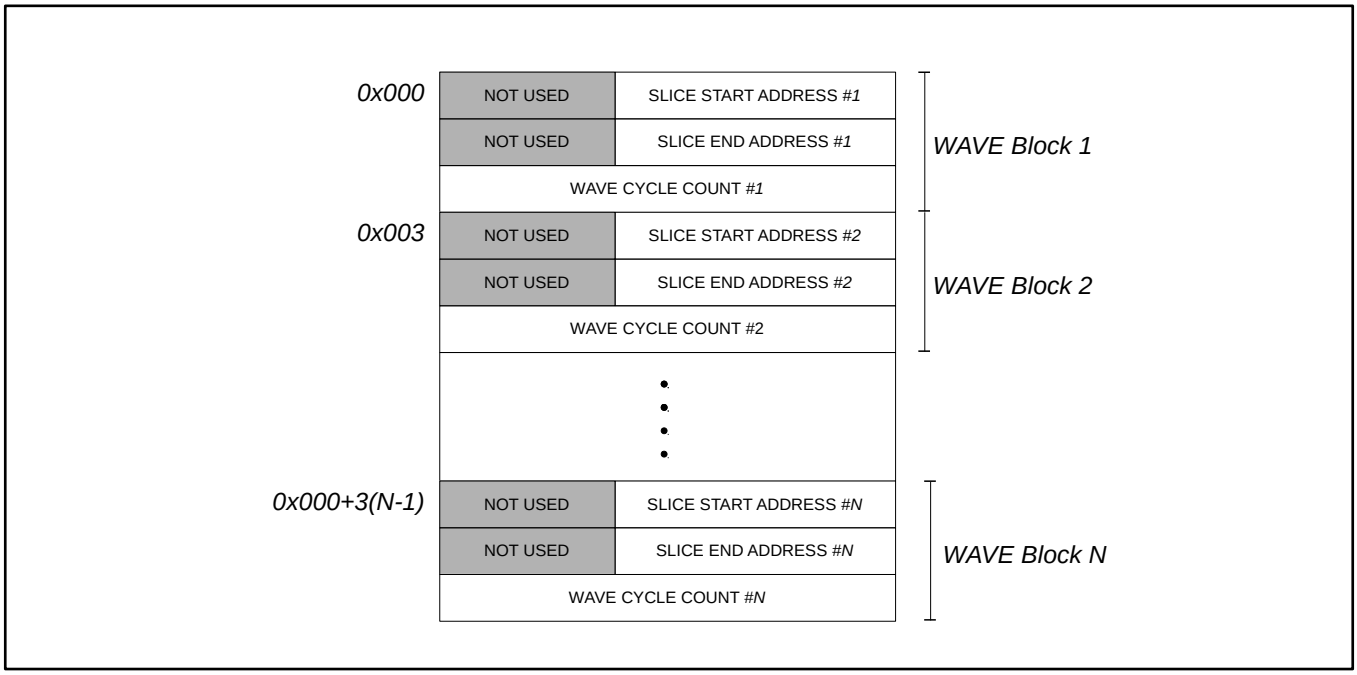


Figure 18: WAVE blocks in RAM

6.8.1.3 Sequencer

The sequencer stores up to 15 WAVEFORM_IDs to be played sequentially. WAVEFORM_ID 0 to 14 are stored into the SEQUENCER using the SEQUENCER WFS command. Each WAVEFORM_ID contains the address in memory of a WAVE block to play. All 15 WAVEFORM_IDs must be written sequentially. WAVEFORM_IDs not used may be filled with any address.

Various sets of waveform sequences can be played. The start and end WAVEFORM_IDs to play are defined using the SEQUENCE START/STOP command. The largest sequence to play covers the 15 WAVEFORM_IDs from WAVEFORM_IDs 0 up to WAVEFORM_IDs 14. The smallest sequence is when the start address is equal to the end address and thus only one WAVEFORM_ID will be played. The Figure 19 shows an example where the waveform starts at WAVEFORM_ID 3 and ends when WAVEFORM_ID 6 has finished playing.

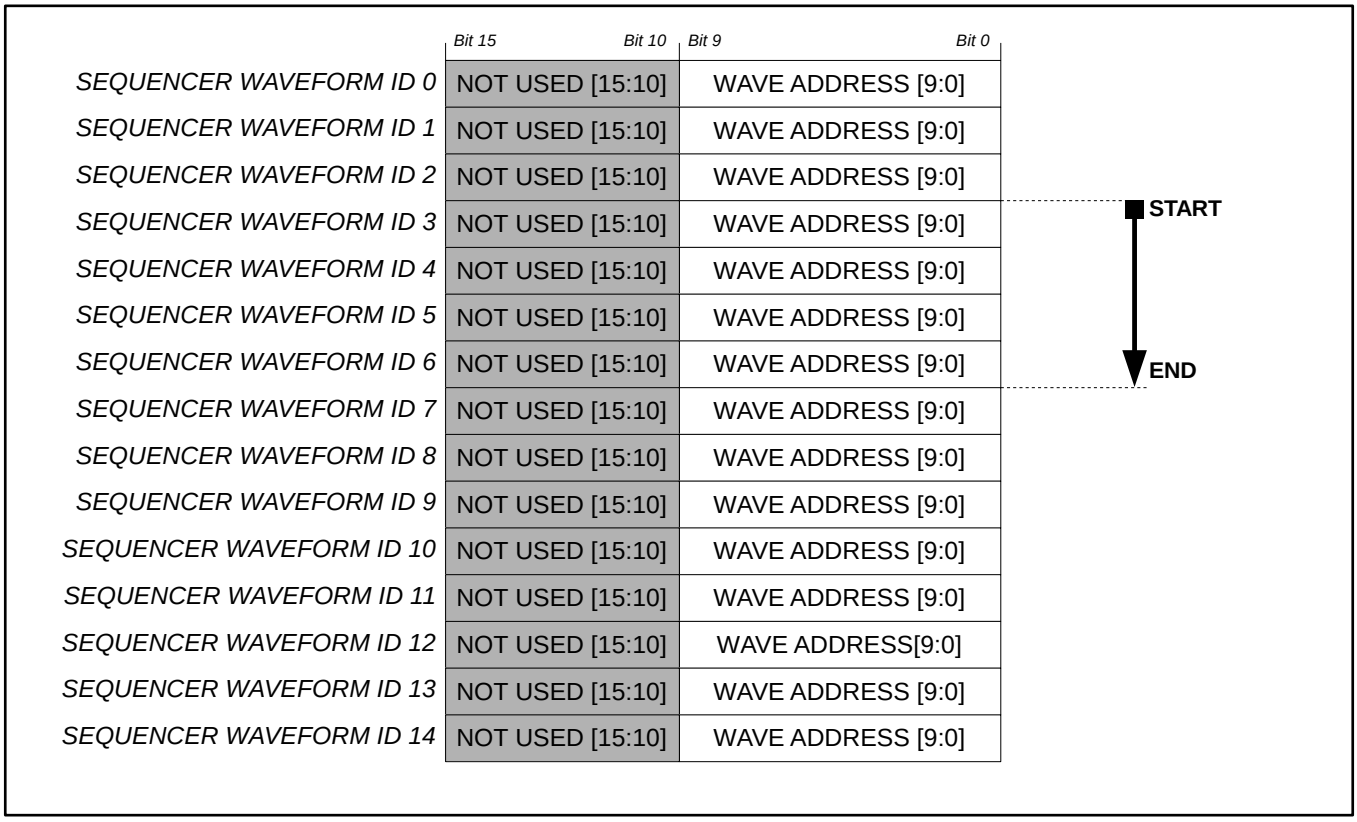


Figure 19: Sequencer example where waveform start at WAVEFORM_ID 3 and ends at 6

6.8.2 Typical Operation Sequence

1. In the RAM register:
    a. Set RAM.MODE[1:0] bits to 0x3 to select RAM synthesis mode.
    b. Set RAM.RAMSEL bit to 0x1 so that subsequent SPI communication is sent to the WFS command interpreter.
2. Write the WAVE blocks and SLICE blocks in the memory using RAM SYNTHESIS WRITE WFS command. Multiple write sequences are needed to program the WAVE(s) and SLICES(s). BURST RAM WRITE WFS command can also be used to write WAVE and SLICE blocks. To keep access to the WFS command interpreter, make sure the commands are sent within 4 µs of each other to continue writing in RAM.
2. Write the WAVEFORM_IDs using the SEQUENCER WFS command with the WAVE blocks RAM address.
3. Write start and end SEQUENCER_Wx that will be played into the SEQUENCE START/STOP WFS command.
4. Wait for more than 4 µs to access to the main register map.
5. Set BC[4:0] to 0xC to output IC_STATUS register content on SDO pin.
6. Set CONFIG.OE bit to 0x1 to enable the haptic waveform generation.
7. Poll EMPTY bit on SDO communication port until it is set to 0x1 and waveform is completed.
8. Set CONFIG.OE bit to 0x0 to deactivate haptic waveform playback.

To start playback with sensing detection, the sensing parameters can be configured between step 4. and 5. See section 6.9 for sensing configuration details.

6.8.3 RAM Synthesis Mode Example

Table 15 and Figure 20 present a waveform playback example using RAM Synthesis mode with 3 SLICES and 2 WAVES. Table 17 is an example where a waveform already programmed in RAM is played.

Table 15: Example of playing a haptic waveform using RAM Synthesis mode

Code	Description
Select RAM Synthesis mode:	
0x8007	Select RAM Synthesis and request access to the WFS command interpreter. The following SPI transactions must be sent less than 4 µs from each other to keep using WFS command interpreter.
Program WAVE #1 in RAM:	
0x0001	Use RAM SYNTHESIS WRITE WFS command.
0x0000	Set the RAM address, where the WAVE #1 will be programmed, to 0x0000.
0x0100	WAVE #1 Data: Set SLICE START ADDRESS to 0x0100 (RAM start address of SLICE #1).
0x0102	WAVE #1 Data: Set SLICE END ADDRESS to 0x0102 (RAM end address of SLICE #1).
0x0001	WAVE #1 Data: Set WAVE CYCLE COUNT to 1.
Program SLICE #1 in RAM:	
0x0001	Use RAM SYNTHESIS WRITE WFS command.
0x0100	Set the RAM address, where the SLICE #1 will be programmed, to 0x0100.
0x0800	SLICE #1 Data: Set AMPLITUDE to 60 V .
0x031A	SLICE #1 Data: Set CYCLES to 3 and FREQUENCY to 101.4 Hz.
0x0020	SLICE #1 Data: Set SHAPEUP[3:0] to 64 ms and SHAPEDN[3:0] to 0 ms.
Program WAVE #2 in RAM:	
0x0001	Use RAM SYNTHESIS WRITE WFS command.
0x0003	Set the RAM address, where the WAVE #2 will be programmed, to 0x0003.
0x0200	WAVE #2 Data: Set SLICE START ADDRESS to 0x0200 (RAM start address of SLICE #2).
0x0205	WAVE #2 Data: Set SLICE END ADDRESS to 0x0205 (RAM end address of SLICE #3).
0x0003	WAVE #2 Data: Set WAVE CYCLE COUNT to 3.
Program SLICE #2 in RAM:	
0x0001	Use RAM SYNTHESIS WRITE WFS command.
0x0200	Set the RAM address, where the SLICE #2 will be programmed, to 0x0200.
0x0AAA	SLICE #2 Data: Set AMPLITUDE to 80 V.
0x020D	SLICE #2 Data: Set CYCLES to 2 and FREQUENCY to 50.7 Hz.
0x0000	SLICE #2 Data: Set SHAPEUP[3:0] to 0 ms and SHAPEDN[3:0] to 0 ms.
Program SLICE #3 in RAM:	
0x0001	Use RAM SYNTHESIS WRITE WFS command.
0x0203	Set the RAM address, where the SLICE #3 will be programmed, to 0x0203.
0x0555	SLICE #3 Data: Set AMPLITUDE to 40 V.
0x0427	SLICE #3 Data: Set CYCLES to 4 and FREQUENCY to 152.1 Hz.
0x0000	SLICE #3 Data: Set SHAPEUP[3:0] to 0 ms and SHAPEDN[3:0] 0 ms.

Code	Description
Program sequencer entries:	
0x0002	Use SEQUENCE WFS command.
0x0000	WAVEFORM_ID 0 value: WAVE #1 block address.
0x0003	WAVEFORM_ID 1 value: WAVE #2 block address.
0x0000	WAVEFORM_ID 2 value: not used.
0x0000	WAVEFORM_ID 3 value: not used.
0x0000	WAVEFORM_ID 4 value: not used.
0x0000	WAVEFORM_ID 5 value: not used.
0x0000	WAVEFORM_ID 6 value: not used.
0x0000	WAVEFORM_ID 7 value: not used.
0x0000	WAVEFORM_ID 8 value: not used.
0x0000	WAVEFORM_ID 9 value: not used.
0x0000	WAVEFORM_ID 10 value: not used.
0x0000	WAVEFORM_ID 11 value: not used.
0x0000	WAVEFORM_ID 12 value: not used.
0x0000	WAVEFORM_ID 13 value: not used.
0x0000	WAVEFORM_ID 14 value: not used.
Set start and end sequencer:	
0x0012	Use SEQUENCE START/STOP WFS command.
0x1000	Set start to WAVEFORM_ID 0 and end to WAVEFORM_ID 2.
Wait for more than 4 µs to access to the main registers.	
Start and stop waveform playback:	
0x9628	Set BC[4:0] to 0xC to output IC_STATUS register content on SDO pin.
0x5010	Set CONFIG.OE to 0x1 to start waveform playback.
0x0000	Poll EMPTY bit on SDO communication port until it is set to 0x1 and waveform is completed.
0x5000	Set OE bit to 0x0 to deactivate haptic waveform playback.

Table 16: Example of playing a haptic waveform already programmed in RAM using RAM Synthesis mode

Code	Description
Set start and end sequencer:	
0x8007	Select RAM Synthesis and request access to the WFS command interpreter. The following SPI transactions must be sent less than 4 µs from each other to keep using WFS command interpreter.
0x0012	Use SEQUENCE START/STOP WFS command.
0x1000	Set start to WAVEFORM_ID 0 and end to WAVEFORM_ID 2.
Wait for more than 4 µs to access to the main registers.	
Start and stop waveform playback:	
0x9628	Set BC[4:0] to 0xC to output IC_STATUS register content on SDO pin.
0x5010	Set OE bit to 0x1 to start haptic waveform playback and PLAY[2:0] to 8 ksps.
0x0000	Poll EMPTY bit on SDO communication port until it is set to 0x1 and waveform is completed.
0x5000	Set OE bit to 0x0 to deactivate haptic waveform playback.

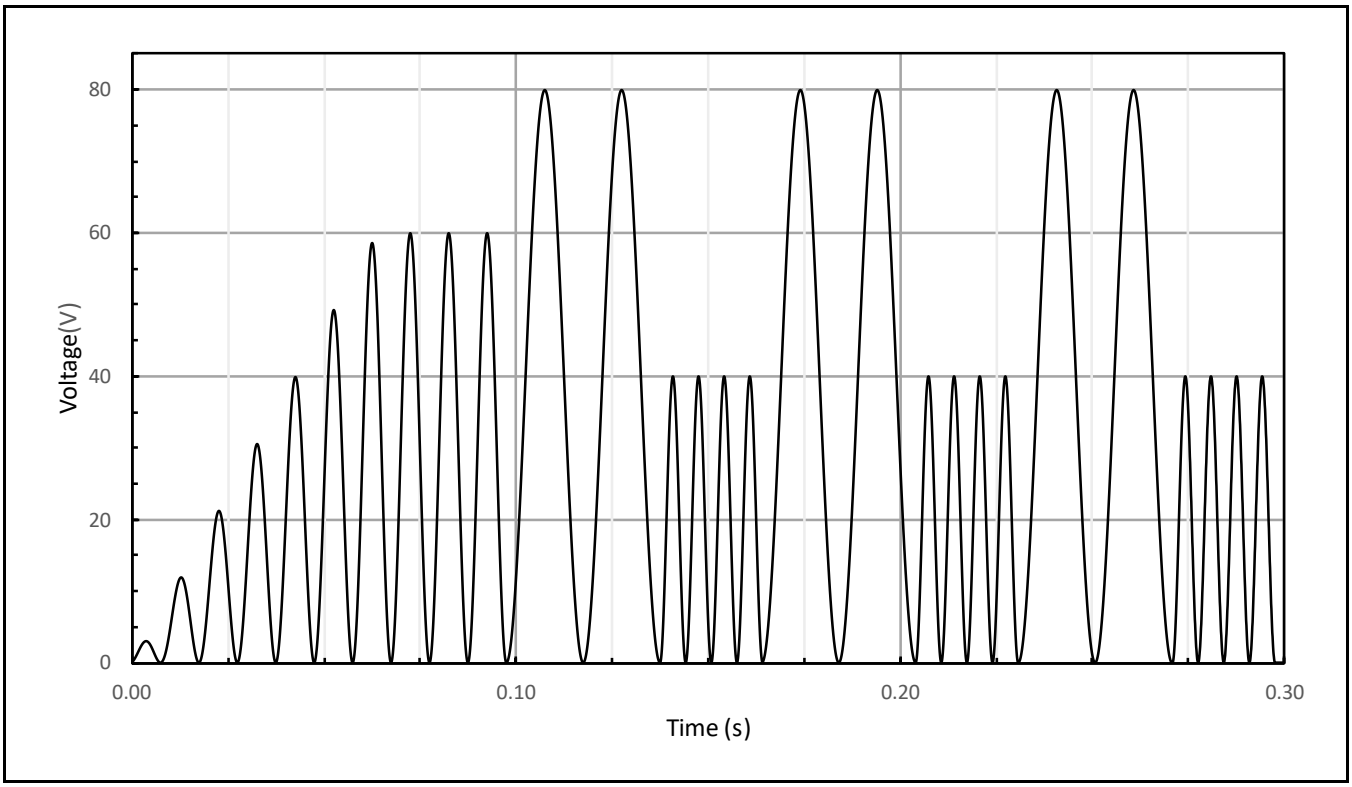


Figure 20: RAM Synthesis waveform example

6.9 Piezo Actuator Sensing

The digital front-end gives access to internal registers 0xA and 0x12 to use the piezo actuator as a force sensor. An embedded comparator can be used to detect when a voltage threshold has been crossed. A waveform may be automatically played with minimum intervention from the MCU. It is also possible to access to the sensed voltage for a custom detection.

The following control bits activate the sensing operation:

- CONFIG.SENSE bit deactivate Q_1 & Q_2 to sense the actuator voltage on pin HV without forcing a voltage on the OUTPUT node. This bit allows the piezo actuator voltage to vary freely as the user physically interacts with it.
- CONFIG.OE bit enables voltage sensing of the HV pin, which is required for the sensing to operate.

Note the following:

- To stop the sensing feature, it is recommended to reset the device using RST bit to reset registers and RAM.
- No haptic waveform should be playing while setting CONFIG.SENSE bit to 0x1. Wait until the IC_STATUS.EMPTY bit is 0x1 before setting CONFIG.SENSE bit to 0x1.
- When sensing is activated, no haptic waveform can be output.

6.9.1 Embedded Sensing Comparator

The embedded sensing parameters are the following:

- ONCOMP bit enables the embedded comparator performing the automatic sensing. It must be set to 0x1 to enable the sensing. Once an event has been detected once, ONCOMP bit must be reset to 0x0 then set again to 0x1 to allow the comparator to detect a second event.
- REP[2:0] bits set the hold time, which is the time the voltage must be above or below the threshold for the detection to be successful.
- STHRESH[8:0] bits set the differential voltage threshold that must be reached for the detection to succeed.
- SIGN bit defines if voltage feedback value should be above or below the threshold to trigger an event from the sense comparator.

6.9.2 GPO Used as Interrupt

The GPO output pin can be used to convey information and implement interrupts for the system with the following configurations:

- Setting GPO[2:0] to 0x1 (SENSE_TRIGGER) will indicate when the embedded sensing (ONCOMP bit set to 0x1) is successful.
- Setting GPO[2:0] to 0x2 (waveform done) will indicate when the waveform playback following a sensing detection event has completed (ONCOMP and AUTO bits set to 0x1).

6.9.3 Automatic Haptic Playback

With the Automatic Haptic Playback, the BOS1211 can detect force applied on a piezo actuator by measuring voltage across its terminal and then automatically play a pre-programmed waveform using RAM Playback (section 6.7) or RAM Synthesis (section 6.8) modes with minimum intervention from the MCU.

The Automatic Haptic Playback is enabled by setting AUTO bit to 0x1. Pin GPO can notify the MCU that both the sensing event and waveform are completed (see section 6.9.2). Once a detection occurs, the automatic playback can be enabled again doing the following:

1. The next waveform should be armed (see section 6.9.3.2 for detail).
2. The sensing comparator should be restarted by first resetting ONCOMP bit to 0x0, and then setting it back to 0x1.

6.9.3.1 Sequence Example for Button Press Sensing with Automatic Playback

A typical communication sequence to configure automatic haptic playback activated by a button press event is as follows:

1. Program waveform using RAM Playback (section 6.7) or RAM Synthesis (section 6.8) modes.
2. Set SPI.GPO[2:0] bits to 0x2 to be notified of a detection event and that waveform completed on the GPO output pin.
3. Write 0xAA07 in the SENSING register to set the following:
    a. SENSING.REP[2:0] bits to 0x5 to set 4096 µs hold time.
    b. SENSING.STHRESH[8:0] bits to 0x7 to set 900 mV threshold.
4. Write 0x5B17 in the CONFIG register to set the following:
    a. CONFIG.SIGN bit to 0x0 to trigger on a voltage above the threshold (detect an increasing voltage).
    b. CONFIG.AUTO bit to 0x1 to play a pre-programmed RAM Playback or RAM Synthesis waveform automatically on a successful detection.
    c. Set CONFIG.ONCOMP bit to 0x1 to enable the embedded sensing comparator.
    d. Set CONFIG.SENSE bit to 0x1 to enable piezo actuator sensing.
    e. Set CONFIG.OE bit to 0x1 to start sensing.

6.9.3.2 Sequence Example for Button Release Sensing with Automatic Playback

Once a detection occurred, sensing can be configured again for automatic haptic playback activated by a button release event using the following typical communication sequence:

1. Set CONFIG.ONCOMP bit to 0x0 to reset the sensing comparator.
2. Arm the next waveform depending on the playback mode:
    a. RAM Playback: write the start and end addresses in the RAM PLAYBACK WFS command (see section 6.7).
    b. RAM Synthesis: write the start and end WAVEFORM_IDs in the SEQUENCE START/STOP WFS command (see section 6.8).
3. Write 0xABFE in the SENSING register to set the following:
    a. SENSING.REP[2:0] bits to 0x5 to set 4096 µs hold time.
    b. SENSING.STHRESH[8:0] bits to 0x1FE to set -260 mV threshold.
4. Write 0x5F17 in the CONFIG register to set the following:
    a. CONFIG.SIGN bit to 0x1 to trigger on voltage below the threshold (detect a decreasing voltage).
    b. CONFIG.AUTO bit to 0x1 to play a pre-programmed RAM Playback or RAM Synthesis waveform automatically on a successful detection.
    c. CONFIG.ONCOMP bit to 0x1 to enable the sensing comparator.
    d. CONFIG.SENSE bit to 0x1 to enable piezo actuator sensing.
    e. CONFIG.OE bit to 0x1 to start sensing.

6.9.4 Reading the Sensed Voltage

The sensed voltage can be read at any time by setting the SDO output using SPI.BC = 0x12. It is seldom read when the embedded sensing feature is used, but it can be read to implement more complex sensing algorithm running in a MCU such as slope detection or voltage profile pattern recognition.

The sensed voltage is continually updated and pushed to the SENSE_VALUE[8:0] field so the last voltage sensed can be read at any time. The RS bit allow to reset the voltage across the piezo actuator as well as the SENSE_VALUE[8:0] bits. Such a reset might be needed if SENSE_VALUE[8:0] is non-zero while the user is not interacting with the actuator.

The following control bits are used to read the sensed voltage:

- SENSE bit in broadcast register 0x12 indicates if the sensing mode is running.
- SENSE_FLAG bit in broadcast register 0x12 indicates if the sensing conditions are met based on CONFIG.SIGN, SENSING.STHRESH[8:0] and SENSING.REP[2:0] bits.
- SENSE_VALUE[8:0] bits is the 9-bit signed sensed voltage.
- RS bit resets the sensing interface without disabling it. This resets the sensing value (SENSE_VALUE[8:0]). The bit self-clears.
- SHORT[1:0] bits determine the time to short the piezo actuator. This occurs periodically while the sensed voltage is negative. The accumulated voltage is output in the sensing value (SENSE_VALUE[8:0] of the broadcast register 0x12). SHORT[1:0] bits are typically set to their default value but may be changed depending on the actuator used and the application conditions.

6.9.4.1 Polling Sequence Example

A typical communication sequence to poll SENSE_VALUE[8:0] is as follows:

1. Write 0x5217 in the CONFIG register to set the following:
    a. CONFIG.ONCOMP bit to 0x0 to prevent it from triggering a sensing event.
    b. CONFIG.SENSE bit to 0x1 to enable piezo actuator sensing.
    c. CONFIG.OE bit to 0x1 to start sensing.
2. Set SPI.BC[4:0] bits to 0x12 to broadcast the SENSE_VALUE[8:0] on SDO.
3. Write a dummy 0xF000 to SPI interface, read a word and extract SENSE_VALUE[8:0] bits to monitor the voltage across the piezo (see section 6.11.17 for more detail on how to use the SDO Broadcast).
4. Repeat the step 3) as needed.

6.10 WFS Command Interpreter

The 1024×16 RAM is programmed using the WFS command interpreter through the REFERENCE register. The WFS commands are also used to store RAM Playback (section 6.7) and RAM Synthesis (section 6.8) configuration data. To access the WFS Command Interpreter, the RAMSEL bit must first be set to 0x1.

WFS commands are summarized in Table 17 and detailed in section 6.10.1.

Table 17: WFS command list summary

COMMAND	WORD	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM SYNTHESIS WRITE	0	COMMAND[15:0] = 0x0001															
	1	RSVD					W/R	ADDRESS[9:0]									
	2	DATA1[15:0]															
	3	DATA2[15:0]															
	4	DATA3[15:0]															
SEQUENCER	0	COMMAND[15:0] = 0x0002															
	1							WAVEFORM ID 0 - WAVE_ADDRESS[9:0]									
	2							WAVEFORM ID 1 - WAVE_ADDRESS[9:0]									
	3							WAVEFORM ID 2 - WAVE_ADDRESS[9:0]									
	4							WAVEFORM ID 3 - WAVE_ADDRESS[9:0]									
	5							WAVEFORM ID 4 - WAVE_ADDRESS[9:0]									
	6							WAVEFORM ID 5 - WAVE_ADDRESS[9:0]									
	7							WAVEFORM ID 6 - WAVE_ADDRESS[9:0]									
	8							WAVEFORM ID 7 - WAVE_ADDRESS[9:0]									
	9							WAVEFORM ID 8 - WAVE_ADDRESS[9:0]									
	10							WAVEFORM ID 9 - WAVE_ADDRESS[9:0]									
	11							WAVEFORM ID 10 - WAVE_ADDRESS[9:0]									
	12							WAVEFORM ID 11 - WAVE_ADDRESS[9:0]									
	13							WAVEFORM ID 12 - WAVE_ADDRESS[9:0]									
	14							WAVEFORM ID 13 - WAVE_ADDRESS[9:0]									
	15							WAVEFORM ID 14 - WAVE_ADDRESS[9:0]									
SEQUENCE START/STOP	0	COMMAND[15:0] = 0x0012															
	1	SEQUENCE END[3:0]				SEQUENCE START[3:0]											
RAM PLAYBACK	0	COMMAND[15:0] = 0x0013															
	1							RAM PLAYBACK ADDRESS START[9:0]									
	2							RAM PLAYBACK ADDRESS END[9:0]									
BURST RAM WRITE	0	COMMAND[15:0] = 0x0014															
	1							BURST START ADDRESS[9:0]									
	2							BURST DATA COUNT[9:0]									
	3	DATA[15:0]															
	…	…															
	2+n	DATAn (n = BURST DATA COUNT[9:0])															
FULL RAM READ	0	COMMAND[15:0] = 0x0015															
FULL RAM READ BREAK	0	COMMAND[15:0] = 0xFF15															

6.10.1 0x0001 RAM SYNTHESIS WRITE

Table 18: RAM SYNTHESIS WRITE command details

ADDRESS: 0x0001 RAM SYNTHESIS WRITE															
Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	COMMAND[15:0] = 0x0001															
1	Not used: 0x0					W/R	ADDRESS[9:0]									
2	DATA1[15:0]															
3	DATA2[15:0]															
4	DATA3[15:0]															

WORD, BITS	NAME	DESCRIPTION
Word 1, Bit [10]	W/R	0: RAM Write Enable 1: RAM Read Enable (SPI.BC[4:0] bits must be set to 0x1C)
Word 1, Bits [9:0]	ADDRESS	Starting RAM address for reading or writing to RAM.
Word 2, Bits [15:0]	DATA1	Data written to RAM at address ADDRESS[9:0]. The word is required if W/R bit is set to 0x0 to enable RAM write.
Word 3, Bits [15:0]	DATA2	Data written to RAM at address ADDRESS[9:0]+1. The word is required if W/R bit is set to 0x0 to enable RAM write.
Word 4, Bits [15:0]	DATA3	Data written to RAM at address ADDRESS[9:0]+2. The word is required if W/R bit is set to 0x0 to enable RAM write.
The RAM SYNTHESIS WRITE register is used to program a WAVE or SLICE block to RAM or read a RAM location. See sections 6.8.1.1 and 6.8.1.2 for details on the content of WAVE and SLICE blocks. Table 15 presents an example on how to write a WAVE and SLICE blocks in RAM. Table 19 presents an example on how to read a RAM location using RAM SYNTHESIS WRITE command.		

Table 19: RAM read sequence example using RAM SYNTHESIS WRITE command

Code	Description
0x9E28	Set SPI.BC[4:0] bits to 0x1C and TE bit to 0x1.
0x8007	Select RAM Synthesis and request access to the WFS command.
0x0001	WFS command: set to RAM SYNTHESIS WRITE.
0x0000	Set RAM address for data reading to 0x0000 and wait for more than 4 µs to access to the main registers.
0x0000	Read 2 bytes corresponding to the content of RAM at address 0x0000.

6.10.2 0x0002 SEQUENCER

Table 20: SEQUENCER command details

	ADDRESS: 0x0002 SEQUENCER															
Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	COMMAND[15:0] = 0x0002															
1	Not used: 0x0						WAVEFORM ID 0 - WAVE_ADDRESS[9:0]									
2	Not used: 0x0						WAVEFORM ID 1 - WAVE_ADDRESS[9:0]									
3	Not used: 0x0						WAVEFORM ID 2 - WAVE_ADDRESS[9:0]									
4	Not used: 0x0						WAVEFORM ID 3 - WAVE_ADDRESS[9:0]									
5	Not used: 0x0						WAVEFORM ID 4 - WAVE_ADDRESS[9:0]									
6	Not used: 0x0						WAVEFORM ID 5 - WAVE_ADDRESS[9:0]									
7	Not used: 0x0						WAVEFORM ID 6 - WAVE_ADDRESS[9:0]									
8	Not used: 0x0						WAVEFORM ID 7 - WAVE_ADDRESS[9:0]									
9	Not used: 0x0						WAVEFORM ID 8 - WAVE_ADDRESS[9:0]									
10	Not used: 0x0						WAVEFORM ID 9 - WAVE_ADDRESS[9:0]									
11	Not used: 0x0						WAVEFORM ID 10 - WAVE_ADDRESS[9:0]									
12	Not used: 0x0						WAVEFORM ID 11 - WAVE_ADDRESS[9:0]									
13	Not used: 0x0						WAVEFORM ID 12 - WAVE_ADDRESS[9:0]									
14	Not used: 0x0						WAVEFORM ID 13 - WAVE_ADDRESS[9:0]									
15	Not used: 0x0						WAVEFORM ID 14 - WAVE_ADDRESS[9:0]									

BIT	NAME	DESCRIPTION
Word 1 to 15, Bits [9:0]	WAVE_ADDRESS	Address of a WAVE block in RAM. The SEQUENCER can store up to 15 different WAVE ADDRESS, named WAVEFORM_ID 0 to WAVEFORM_ID 14.

The SEQUENCER is composed of 15 WAVEFORM_ID numbered 0x0 to 0xE (WAVEFORM_ID 0 to WAVEFORM_ID 14). Each WAVEFORM_ID contains a RAM address of a WAVE block.

Table 15 presents an example on how to use SEQUENCE command.

Note that all 15 WAVEFORM_ID must be written. The WAVEFORM_ID registers that are not used may be assigned to any value.

6.10.3 0x0012 SEQUENCE START/STOP

Table 21: SEQUENCE START/STOP command details

	ADDRESS: 0x0012 SEQUENCE START/STOP															
Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	COMMAND[15:0] = 0x0012															
1	SEQUENCE END[3:0]				SEQUENCE START[3:0]				Not used: 0x0							

BIT	NAME	TYPE	DESCRIPTION
Word 1, Bits [15:12]	SEQUENCE END	W	Set the SEQUENCER end WAVEFORM_ID number (numbered 0x0 to 0xE, see SEQUENCER register) pointing to the last WAVE block to play.
Word 1, Bits [11:8]	SEQUENCE START	W	Set the SEQUENCER start WAVEFORM_ID number (numbered 0x0 to 0xE, see SEQUENCER register) pointing to the first WAVE block to play.

The SEQUENCER will play all WAVE blocks starting from SEQUENCE START[3:0] up to SEQUENCE_END[3:0].

Using SEQUENCE START/STOP command indicates that the waveform specified from SEQUENCE START to SEQUENCE END is armed and ready to be played.

Table 15 presents an example on how to use SEQUENCE START/STOP command.

6.10.4 0x0013 RAM PLAYBACK

Table 22: RAM PLAYBACK command details

	ADDRESS: 0x0013 RAM PLAYBACK															
Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	COMMAND[15:0] = 0x0013															
1	Not used: 0x0						RAM PLAYBACK ADDRESS START[9:0]									
2	Not used: 0x0						RAM PLAYBACK ADDRESS END[9:0]									

BIT	NAME	TYPE	DESCRIPTION
Word 1, Bits [9:0]	RAM PLAYBACK ADDRESS START	W	Defines the starting address for fetching RAM Playback samples.
Word 2, Bits [9:0]	RAM PLAYBACK ADDRESS END	W	Defines the address of the last sample read during playback.

The start and end addresses of the RAM PLAYBACK register indicate the location in RAM of the samples to be fetched when RAM Playback is initiated. The samples in RAM can be set using BURST RAM WRITE register with the same format as the REFERENCE register.

Using RAM PLAYBACK command indicates that the waveform specified RAM PLAYBACK ADDRESS START[9:0] and RAM PLAYBACK ADDRESS END[9:0] is ready to be played.

Table 11 presents an example on how to use RAM PLAYBACK command.

6.10.5 0x0014 BURST RAM WRITE

Table 23: BURST RAM WRITE command details

	ADDRESS: 0x0014 BURST RAM WRITE															
Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	COMMAND[15:0] = 0x0014															
1	Not used: 0x0						START ADDRESS[9:0]									
2	Not used: 0x0						DATA COUNT[9:0]									
3	DATA[15:0]															

BIT	NAME	TYPE	DESCRIPTION
Word 1, Bits [9:0]	START ADDRESS	W	RAM address from where to start writing.
Word 2, Bits [9:0]	DATA COUNT	W	The number of data words to be written on RAM with the following constraints: DATA COUNT value of 0 will be considered as 1024 (all RAM locations). DATA COUNT ≤ (1024 – START ADDRESS[9:0])
Word 3, Bits [15:0]	DATA	W	Data to be written in RAM. DATA[15:0]. The RAM write address is incremented automatically between each written word.

BURST RAM WRITE is used to write multiple words to RAM. Words can be any data for RAM Playback mode (see section 6.7) or RAM Synthesis such as WAVE and SLICE blocks (see section 6.8).

Table 11 presents an example on how to use BURST RAM WRITE command.

6.10.6 0x0015 FULL RAM READ

Table 24: FULL RAM READ command

	COMMAND: 0x0015 FULL RAM READ															
Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	COMMAND[15:0] = 0x0015															

Prior using FULL RAM READ command, SPI.BC[4:0] bits must be set to 0x1C. Once 0x0015 is set, the full RAM content can be read on the communication interface, starting at the RAM address = 0x000, with the address self-incrementing after each read until one of the following conditions occurs:

- All 1024 addresses have been read
- FULL RAM READ BREAK command is sent
- 4 µs timeout occurs between each read.

The communication sequence to use the FULL RAM READ command includes the following:

1. Write 0x8006 to set RAM.RAMSEL to 0x1 and RAM.MODE to 0x10 to select RAM PLAYBACK mode.
2. Write 0x9E28 to set SPI.BC[4:0] bits to 0x1C and output the RAM content on SDO pin.
3. Write 0x0015 on SPI communication bus to use the FULL RAM READ command.
4. Wait at least 500 ns and less than 4 µs.
5. Make a single dummy write using 0x0000 on SPI communication.
6. Wait a minimum of 500 ns
7. Make one dummy write using 0x000 and read one word on SPO pin.
8. Repeat steps 4) and 5) until the last RAM address.

6.10.7 0xFF15 FULL RAM READ BREAK

Table 25: FULL RAM READ BREAK command

	COMMAND: 0xFF15 FULL RAM READ BREAK															
Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	COMMAND[15:0] = 0xFF15															
	The FULL RAM READ BREAK command 0xFF15 is used to stop the RAM content reading loop started with the FULL RAM READ command.															

6.11 Main Register Map

Table 26 lists the main register map used to configure the BOS1211 and Table 27 lists registers accessible for reading with SPI.BC[4:0] register. Access to the WFS command interpreter requires RAMSEL bit set to 0x1.

Table 26: Main register map

ADDRESS [15:12]	NAME	DEFAULT VALUE	R/W[3]	11	10	9	8	7	6	5	4	3	2	1	0
0x0	REFERENCE	0x000	RW	REFERENCE[11:0]											
0x1	ION_BL	0x11C	RW	FSWMAX[1:0]		SB[1:0]		I_ON_SCALE[7:0]							
0x2	DEADTIME	0x46A	RW	DHS[6:0]							DLS[4:0]				
0x3	KP	0x080	RW	SQ	KP[10:0]										
0x4	KPA_KI	0x310	RW	KIBASE[3:0]				KPA[7:0]							
0x5	CONFIG	0x000	RW	ONCOMP	SIGN	SENSE	AUTO	SYNC	LOCK	RST	OE	DS	PLAY[2:0]		
0x6	PARCAP	0x00A	RW	SHS[1:0]		SLS[1:0]		PARCAP[7:0]							
0x7	SUP_RISE	0x5CF	RW	TOUT	VIN[4:0]					TI_RISE[5:0]					
0x8	RAM	0x001	RW	RSVD									RAM_SEL	MODE[1:0]	
0x9	SPI	0x7A8	RW	BC[4:0]					SHORT[1:0]		RS	TE	GPO[2:0]		
0xA	SENSING	0x000	RW	REP[2:0]				STHRESH[8:0]							
0xB	THRESHOLD	0x048	RW	VTHRESH[8:0]									THRESH_ERROR[2:0]		
0xC	IC_STATUS	0x001	RW	STATE[1:0]		OVV	OVT	MXPWR	IDAC	UVLO5	UVLO12	OVLO12	SC	FULL	EMPTY
0xD	FIFO_STATUS	0x400	RW	ERROR	EMPTY	FIFO_SPACE[9:0]									
0xE	TRIM	0x000	RW	TRIMRW[1:0]		TRIM_OSC[6:0]							TRIM_REG[2:0]		
0xF	CHIP_ID	0x034	RW	RSVD						CHIP ID[5:0]					

Table 27: Extra broadcast register map

ADDRESS IN SPI.BC [4:0]	NAME	R/W[1]	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0 to 0xF		RO	BC[3:0]				Content of main register with address BC[3:0]											
0x10	VFEEDBACK	RO	RSVD				STATE[1:0]		VFEEDBACK[9:0]									
0x11	OFFSET	RO	RSVD						OFFSET [9:0]									
0x12	SENSE_STATUS	RO	RSVD					SENSE	SENSE_ FLAG	SENSE_VALUE[8:0]								
0x1C	RAM_DATA	RO	RAM_DATA_RAW[15:0]															

[3] RO are read-only registers.
RW are read/write registers.

6.11.1 0x0 REFERENCE

Table 28: REFERENCE register details

ADDRESS: 0x0	REFERENCE					DEFAULT:0x000					
11	10	9	8	7	6	5	4	3	2	1	0
REFERENCE[11:0]											

Bits	Name	Default	Type	Description
11:0	REFERENCE	0x00	R/W	In Direct or FIFO mode (MODE[1:0] bits set to 0x0 or 0x1), REFERENCE[11:0] defines the OUTPUT node amplitude in 12-bit unsigned format. The relation between REFERENCE[11:0] and output amplitude (OUTPUT) in volt is determined by: $$REFERENCE\ [11:0] = \text{OUTPUT} \times 30.74$$ REFERENCE[11:0] should not exceed 3689 to keep the voltage sensed on HV pin ≤120 V. In RAM PLAYBACK or RAM SYNTHESIS mode (MODE[1:0] bits set to 0x2 or 0x3), REFERENCE[11:0] defines the WFS commands (see section 6.10 for details).

6.11.2 0x1 ION_BL

Table 29: ION_BL register details

ADDRESS: 0x1	ION_BL					DEFAULT:0x11C					
11	10	9	8	7	6	5	4	3	2	1	0
FSWMAX[1:0]		SB[1:0]		IONSCALE[7:0]							

Bits	Name	Default	Type	Description
11:10	FSWMAX	0x0	R/W	Boost converter maximum switching frequency. 0x0: 1 MHz 0x1: 833 kHz 0x2: 666 kHz 0x3: 500 kHz
9:8	SB	0x1	R/W	Boost converter blanking time. 0x0: 70 ns 0x1: 88 ns 0x2: 106 ns 0x3: 124 ns Default value should work for all applications.
7:0	IONSCALE	0x1C	R/W	Minimum current required to turn on high-side switch (Q2). IONSCALE[7:0] must be determined by: $$IONSCALE[7:0] = round\left(\frac{R_{sense}}{150 \times L_1}\right)$$

6.11.3 0x2 DEADTIME

Table 30: DEADTIME register details

ADDRESS: 0x2	DEADTIME						DEFAULT:0x46A				
11	10	9	8	7	6	5	4	3	2	1	0
DHS[6:0]							DLS[4:0]				

Bits	Name	Default	Type	Description
11:5	DHS	0x23	R/W	Defines t_{Q1-Q2}, which is the minimum time between low-side switch (Q_1) turns off and high-side switch (Q_2) turns on. t_{Q1-Q2} is determined by: $$t_{Q1-Q2} = DHS \times 1.1\ ns$$ DHS [6:0] is determined by: $$DHS[6:0] = \frac{2\pi\sqrt{L_1 \times \left(C_{oss-Q1} + C_{oss-Q2} + C_{par}\right)}}{4 \times 1.1 \times 10^{-9}}$$ Where C_{OSS-Q1} and C_{OSS-Q2} are the output capacitance of the power transistors Q_1 and Q_2 and C_{par} is the parasitic capacitance seen on pin SW which includes the parasitic capacitance of inductor (L_1) and PCB layout. DHS[6:0] can be optimized for specific applications.
4:0	DLS	0x0A	R/W	Defines the minimum time between high-side switch (Q_2) turn off and low-side switch (Q_1) turn on (t_{Q2-Q1}). The relation between t_{Q2-Q1} in second and DHS[4:0] is determined by: $$DLS[4:0] = \frac{t_{Q2-Q1}}{4.4 \times 10^{-9}}$$ Default value provides a delay of 46 ns minimum and should work for most applications but DLS[4:0] can be optimized for specific applications.

6.11.4 0x3 KP

Table 31: KP register details

ADDRESS: 0x3	KP						DEFAULT:0x080				
11	10	9	8	7	6	5	4	3	2	1	0
SQ	KP[10:0]										

Bits	Name	Default	Type	Description
11	SQ	0x0	R/W	Allows the user to safely send discontinuous waveforms with arbitrary sample rate. As soon as a sample is received, the OUTPUT node voltage will start to move toward the new value. 1: Square waves (not recommended for typical applications) 0: Continuous waveforms
10:0	KP	0x080	R/W	Sets the physical value ($k_{Physical}$) of the integrated PI controller proportional gain. $K_{pPhysical}$ in A/V is determined by: $$Kp_{physical} = \frac{KP[10:0]\ \times 2^{-14}}{R_{sense}}$$

6.11.5 0x4 KP

Table 32: KPA_KI register details

ADDRESS: 0x4	KPA_KI					DEFAULT:0x310					
11	10	9	8	7	6	5	4	3	2	1	0
KIBASE[3:0]				KPA[7:0]							

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11:8	KIBASE	0x3	R/W	Determines the pole location (f_{pole}) of the integrated PI controller. The pole location (f_{pole}) in kHz is determined by: $$f_{pole} = \frac{1024}{2^{KIBASE}}$$
7:0	KPA	0x10	R/W	Determines the proportional gain (KPc) used in the integrated PI controller. KPc is calculated by: $$KPc = KP[10:0] + KPA[7:0] \times \text{REFERENCE}[11:0]$$

6.11.6 0x5 CONFIG

Table 33: CONFIG register details

ADDRESS: 0x5	CONFIG					DEFAULT:0x000					
11	10	9	8	7	6	5	4	3	2	1	0
ONCOMP	SIGN	SENSE	AUTO	SYNC	LOCK	RST	OE	DS	PLAY[2:0]		

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11	ONCOMP	0x0	R/W	Enables sensing comparator used use to trigger sensing detection event. ONCOMP bit needs to be reset to 0x0 to clear SENSE_FLAG bit after a detection. 0x1: Comparator active 0x0: Comparator inactive
10	SIGN	0x0	R/W	Defines if SENSE_VALUE[8:0] should be above or below the threshold set by STHRESH[8:0] bits to trigger a sensing detection event. 0x1: Below 0x0: Above
9	SENSE	0x0	R/W	Disables Q_1 and Q_2 to set OUTPUT node to high impedance, enables piezo sensing and push voltage detected on piezo in SENSE_VALUE[8:0] field. ONCOMP, SIGN, AUTO, REP and STHRESH[8:0] fields have no effect if SENSE is set to 0x0. A successful sensing detection clears SENSE bit if AUTO bit is set to 0x1. The waveform must be finished playing before enabling SENSE bit. 0x1: Enable 0x0: Disable

ADDRESS: 0x5	CONFIG				DEFAULT:0x000						
11	10	9	8	7	6	5	4	3	2	1	0
ONCOMP	SIGN	SENSE	AUTO	SYNC	LOCK	RST	OE	DS	PLAY[2:0]		

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
8	AUTO	0x0	R/W	Enables a waveform programmed using RAM Playback or RAM Synthesis to be played automatically when the sensing comparator detect a signal meeting the conditions defined by STHRESH[8:0] and SIGN fields. Auto bit self-clears when the output waveform has finished playing. 0x0: Disable 0x1: Enable
7	SYNC	0x0	R/W	Activate multi-chip synchronization. 0x0: Disable 0x1: Enable
6	LOCK	0x0	R/W	Enable write protections on all registers except CONFIG and REFERENCE registers when OE bit is set to 0x1. 0x0: Disable register write protection 0x1: Enable register write protection
5	RST	0x0	R/W	Software reset. The controller resets internal registers to default values and goes to the IDLE state. RST self-clears once the reset is completed. 0x0: Normal operation 0x1: RESET
4	OE	0x0	RW	Activate haptic waveform playback or piezo actuator sensing. 0x0: Disable 0x1: Enable
3	DS	0x0	RW	Power mode when OE is set to 0x0. In SLEEP, registers and RAM data are are reset. 0x0: IDLE 0x1: SLEEP
2:0	PLAY	0x0	RW	Sets the waveform playback sampling rate when using Direct, FIFO or RAM Playback mode. 0x0: 1024 ksps 0x1: 512 ksps 0x2: 256 ksps 0x3: 128 ksps 0x4: 64 ksps 0x5: 32 ksps 0x6: 16 ksps 0x7: 8 ksps

6.11.7 0x6 PARCAP

Table 34: PARCAP register details

ADDRESS: 0x6		PARCAP						DEFAULT:0x00A			
11	10	9	8	7	6	5	4	3	2	1	0
SHS[1:0]		SLS[1:0]		PARCAP[7:0]							

Bits	Name	Default	Type	Description
11:10	SHS	0x0	R/W	Sets high-side gate driver strength based on transistor Q_2 used (see section 7.4.5). Default value should work with C_{ISS} of Q_2 of ≤ 2 nF. An increase in SHS reduces the rise and fall time of the GDHS signal, at the cost of increasing EMI and noise. Source / Sink 0x0 : 250 mA / 170 mA 0x1 : 500 mA / 340 mA 0x2 : 825 mA / 550 mA 0x3 : 1100 mA / 800 mA
9:8	SLS	0x0	R/W	Sets low-side gate driver strength based on transistor Q_1 used (see section 7.4.5). Default value should work with C_{ISS} of Q_1 of ≤ 2 nF. An increase in SLS reduces the rise and fall time of the GDLS signal, at the cost of increasing EMI and noise. Source / Sink 0x0: 250 mA / 200 mA 0x1: 500 mA / 380 mA 0x2: 850 mA / 620 mA 0x3: 1200 mA / 850 mA
7:0	PARCAP	0x0A	R/W	Internal parameter determined by: $$PARCAP[7:0] = \sqrt{\frac{C_{oss-Q1} + C_{oss-Q2} + C_{par}}{L}} \times R_{sense} \times 2^{16}$$ Where C_{OSS-Q1} and C_{OSS-Q2} are the output capacitance of Q_1 and Q_2 transistors and C_{par} is the parasitic capacitance seen on pin SW which depends on inductor (L_1) and PCB layout. Typically, the optimal setting for a system is 20% to 50% higher than the calculated value.

6.11.8 0x7 SUP_RISE

Table 35: SUP_RISE register details

ADDRESS: 0x7	SUP_RISE					DEFAULT:0x5CF					
11	10	9	8	7	6	5	4	3	2	1	0
TOUT	VIN[4:0]					TI_RISE[5:0]					

Bits	Name	Default	Type	Description
11	TOUT	0x0	R/W	Timeout in Direct mode and FIFO mode. If TOUT is set to 0x1, EMPTY bit is set to 0x1 and no new data has been received for more than 4 ms, the device automatically goes to SLEEP state. RAM and registers are reset, except PLAY[2:0] bits are set to 0x7. 0x0: Timeout disabled 0x1: Timeout enabled
10:6	VIN	0x17	R/W	Digital representation of the supply voltage V_{IN}. VIN[4:0] is determined by the following: $$\text{VIN}\ [4:0] = \frac{V_{IN}}{0.52}$$ Where, V_{IN} is the supply voltage in volt and 0x11 ≤ VIN[4:0] ≤ 0x1F.
5:0	TI_RISE	0x0F	R/W	Proportional gain for the offset, which is determined by: $$\text{TI\_RISE}[5:0] = \frac{R_{sense}}{428.9 \times L_1}$$

6.11.9 0x8 RAM

Table 36: RAM register details

ADDRESS: 0x8	RAM					DEFAULT:0x001					
11	10	9	8	7	6	5	4	3	2	1	0
RSVD									RAMSEL	MODE[1:0]	

Bits	Name	Default	Type	Description
2	RAMSEL	0x0	R/W	Defines whether SPI communication is transmitted to the WFS command interpreter or to the main register map bank. RAMSEL bit self-clears 4 us after last SPI communication and when the CS pin is back to logic 1. If the CS pin remains at a logic 0, RAMSEL bit doesn't self-clears. 0x0: Communication is transmitted to the main register map bank. 0x1: Communication is transmitted to the WFS command interpreter.
1:0	MODE [1:0]	0x1	R/W	Define waveform playback mode. This register can only be modified if OE bit is set to 0x0. 0x0: Direct mode 0x1: FIFO mode 0x2: RAM Playback 0x3: RAM Synthesis

6.11.10 0x9 SPI

Table 37: SPI register details

ADDRESS: 0x9 SPI							DEFAULT:0x7A8				
11	10	9	8	7	6	5	4	3	2	1	0
BC[4:0]					SHORT[1:0]		RS	TE	GPO[2:0]		

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11:7	BC	0x0F	R/W	Address of internal register whose content is output on SPI port (SDO pin). See section 6.11.17 for details.
6:5	SHORT	0x1	R/W	Defined the length of time the piezo is periodically shorted during sensing (section 6.9). SHORT bit also defines the duration of the piezo zeroing during auto-calibration when OE bit is set to 0x1. 0x0: 500 µs 0x1: 1000 µs 0x2: 1500 µs 0x3: 2000 µs
4	RS	0x0	R/W	Resets SENSE_VALUE[8:0] fields. RS bit self-clears. 0x0: No effect 0x1: Reset sensing interface
3	TE	0x1	R/W	Transmit Enable. 0x0: SDO pin is disabled and forced to 0 V during a transmission 0x1: The device can transmit data on the SDO pin
2:0	GPO	0x0	R/W	Determines the output signal on GPO pin. 0x0: nternal reset. When the device is ready to receive the first communication after power-up, the output will be set to a logic 1. Note that during power-up, the GPO pin will go briefly to 1 during internal calibration and the device will then automatically go to SLEEP state. 0x1: Sense Trigger: Indicates if SENSE_VALUE[8:0] met the threshold detection conditions. Same as the state of SENSE_FLAG bit. 0: Signal on the piezo doesn`t meet the threshold set 1: Signal on piezo meets the threshold set (STHRESH[8:0]) 0x2: Waveform done and FIFO empty: Same as the EMPTY bit state. 0: Data available to play 1: No more data to play 0x3: Error. (Any type of faults): 0: No error detected 1: An error was detected 0x4: MXPWR: 0: Amount of power is acceptable 1: Maximum power, the waveform is likely distorted 0x7: NEXT_DATA. Use in Direct mode (MODE[1:0] = 0x0) 0: No data required from MCU 1: Next data required from MCU

6.11.11 0xA SENSING

Table 38: SENSING register details

ADDRESS: 0xA SENSING											DEFAULT:0x000
11	10	9	8	7	6	5	4	3	2	1	0
REP[2:0]			STHRESH[8:0]								

Bits	Name	Default	Type	Description
11:9	REP	0x0	R/W	Length of time during which the sensed voltage must be ≥ STHRESH[8:0] or ≤ STHRESH[8:0], depending on the SIGN bit. 0x0:1 µs 0x1:15 µs 0x2: 500 µs 0x3: 1000 µs 0x4: 2000 µs 0x5: 4000 µs 0x6: 8000 µs 0x7: 16000 µs
8:0	STHRESH	0x0	R/W	Differential voltage reference in signed decimal value of the sensing comparator, which is required to detect a sensing event and notify the user. STHRESH[8:0] must be different than 0x0 otherwise no comparison is made. The relation between the threshold voltage amplitude (V_{th}) in volts and STHRESH[8:0] is determined by: $$\text{STHRESH}\,[8:0] = V_{th} \times 7.68$$

6.11.12 0xB THRESH

Table 39: THRESH register details

ADDRESS: 0xB THRESH											DEFAULT:0x048
11	10	9	8	7	6	5	4	3	2	1	0
VTHRESH[6:0]							THRESH_ERROR[4:0]				

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11:5	VTHRESH	0x10	R/W	Determine the threshold voltage (V_{th}), below which the error between the output voltage and the setpoint must be to trigger a transition boost-to-buck. The boost-to-buck transition occurs after a delay determined by THRESH_ERROR[4:0]. VTHRESH[6:0] is determined by: $$\text{VTHRESH}\,[6:0] = -V_{th} \times 30.7$$ This register may need to be optimized depending on the actuator characteristics and the presence of an output filter. A small VTHRESH[6:0] value results in rapid boost-to-buck transitions and can lead to discontinuities at the top of the output waveform. A high value results in a delay before the boost-to-buck transition and can lead to flattening at the top of the output waveform.

ADDRESS: 0xB	THRESH						DEFAULT:0x048				
11	10	9	8	7	6	5	4	3	2	1	0
VTHRESH[6:0]							THRESH_ERROR[4:0]				

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
4:0	THRESH_ ERROR	0x08	R/W	Represents the amount of time the error between the output voltage and the setpoint must be less than the threshold voltage set by VTHRESH[6:0] to trigger a boost-to-buck transition. This register may need to be optimized depending on the actuator characteristics and the presence of an output filter. A small THRESH_ERROR[4:0] value results in rapid boost-to-buck transitions and can lead to discontinuities at the top of the output waveform. A high value results in a delay before the boost-to-buck transition and can lead to flattening at the top of the output waveform.

6.11.13 0xC IC_STATUS

Table 40: IC_STATUS register details

ADDRESS: 0xC	IC_STATUS (read-only)						DEFAULT:0x001				
11	10	9	8	7	6	5	4	3	2	1	0
STATE[1:0]		OVV	OVT	MXPWR	IDAC	UVLO5	UVLO12	OVLO12	SC	FULL	EMPTY

Bits	Name	Default	Type	Description
11:10	STATE	0x0	R	STATE of the controller. 0x0: IDLE 0x1: CALIBRATION 0x2: RUN 0x3: ERROR
9	OVV	0x0	R	Over voltage bit. 0x0: Pin HV voltage is OK 0x1: Pin HV voltage exceeded the maximum voltage allowed
8	OVT	0x0	R	Overtemperature status bit. 0x0: IC temperature is OK 0x1: Overtemperature detected on the IC
7	MXPWR	0x0	R	Device is processing maximum amount of power. 0x0: Amount of power is acceptable 0x1: Maximum power, distortion likely
6	IDAC	0x0	R	IDAC status bit. 0x0: No problem with current detection 0x1: Problem with current detection
5	UVLO5	0x0	R	UVLO 5 V status bit. Voltage at VDD pin is too low for proper operation of haptic feedback. 0x0: V_{DD} is OK 0x1: V_{DD} voltage < 4.4 V

ADDRESS: 0xC		IC_STATUS (read-only)					DEFAULT:0x001				
11	10	9	8	7	6	5	4	3	2	1	0
STATE[1:0]		OVV	OVT	MXPWR	IDAC	UVLO5	UVLO12	OVLO12	SC	FULL	EMPTY

Bits	Name	Default	Type	Description
4	UVLO12	0x0	R	UVLO 12 V status bit. Voltage at VIN/RP pin is too low for proper operation of haptic feedback. 0x0: V_{IN} voltage is OK 0x1: V_{IN} voltage < 8.8 V
3	OVLO12	0x0	R	OVLO 12 V status bit. Voltage at VIN/RP pin is too high for proper operation of haptic feedback. 0x0: V_{IN} voltage is OK 0x1: V_{IN} voltage >19.9 V
2	SC	0x0	R	Short circuit status bit. 0x0: IC is OK 0x1: Short circuit detected between OUTPUT and V_{IN}
1	FULL	0x0	R	The FIFO is full. 0x0: Not Full 0x1: Full
0	EMPTY	0x1	R	Waveform playback multi-function status bit. Its function depends on Mode[1:0] bits. In Direct mode (Mode[1:0] bits set to 0x0), EMPTY indicates when new data is needed: 0x0: No sample required 0x1: Next sample required In FIFO mode (Mode[1:0] bits set to 0x1), EMPTY indicates when FIFO is empty: 0x0: FIFO is not empty 0x1: FIFO is empty In RAM Synthesis or RAM Playback modes (Mode[1:0] bits set to 0x2 or 0x3), EMPTY indicates when the haptic waveform has finished playing: 0x0: Waveform is not completed 0x1: Waveform is completed

6.11.14 0xD FIFO_STATUS

Table 41: FIFO_STATUS register details

ADDRESS: 0xD		FIFO_STATUS (read-only)					DEFAULT:0x400				
11	10	9	8	7	6	5	4	3	2	1	0
ERROR	EMPTY	FIFO_SPACE[9:0]									

Bits	Name	Default	Type	Description
11	ERROR	0x0	R	Indicates that an error occurred (any type of faults). 0x0: No error 0x1: An error has occurred

ADDRESS: 0xD		FIFO_STATUS (read-only)					DEFAULT:0x400				
11	10	9	8	7	6	5	4	3	2	1	0
ERROR	EMPTY	FIFO_SPACE[9:0]									

Bits	Name	Default	Type	Description
10	EMPTY	0x1	R	Waveform playback multi-function status bit. Its function depends on Mode[1:0] bits. In Direct mode (Mode[1:0] bits set to 0x0), EMPTY indicates when new data is needed: 0x0: No sample required 0x1: Next sample required In FIFO mode (Mode[1:0] bits set to 0x1), EMPTY indicates when FIFO is empty: 0x0: FIFO is not empty 0x1: FIFO is empty In RAM Synthesis or RAM Playback modes (Mode[1:0] bits set to 0x2 or 0x3), EMPTY indicates when the haptic waveform has finished playing: 0x0: Waveform is not completed 0x1: Waveform is completed
9:0	FIFO_SPACE	0x000	R	Space available in the FIFO for new data. A value of 0x000 with EMPTY bit equal to 0x1 indicates that all the FIFO locations are available. A value of 0x000 with EMPTY bit equals to 0x0 indicates that none of the FIFO locations are available, and the FIFO is full.

6.11.15 0xE TRIM

Table 42: TRIM register details

ADDRESS: 0xE TRIM									DEFAULT:0x000		
11	10	9	8	7	6	5	4	3	2	1	0
TRIMRW[1:0]		TRIM_OSC[6:0]							TRIM_REG[2:0]		

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11:10	TRIMRW	0x0	R/W	Trim control bits for adjusting the internal clock oscillator frequency (TRIM_OSC[6:0]) and 1.8 V internal regulator voltage (TRIM_REG[2:0]), see Figure 21. Hardware fuses values vary from chip-to-chip. More detail is available in section 6.2.11. TRIMRW[1:0] bits are automatically reset to 0x0 after each operation. 0x0: Default behaviour where Hardware fuses are latched to the Trim Block at power-up 0x1: Resets the Trim Block with the Hardware Fuses and then transfers Trim Block data to TRIM_OSC[6:0] and TRIM_REG[2:0] for reading (wait for 1 ms before reading) 0x2: Transfers Trim Block data to TRIM_OSC[6:0] and TRIM_REG[2:0] for reading (wait for 1 ms before reading) 0x3: Writes TRIM_OSC[6:0] and TRIM_REG[2:0] to Trim Block and transfers back Trim Block data to TRIM_OSC[6:0] and TRIM_REG[2:0] for reading (wait for 1 ms before reading)
9:3	TRIM_OSC	0x00	R/W	Oscillator trimming bits in two's complement. The step size is approximately 120 kHz. Maximum frequency at 0x3F. Minimum frequency at 0x40. Excessive change in oscillator frequency may induce circuit malfunction. This is an advanced feature.
2:0	TRIM_REG	0x0	R/W	1.8 V Regulator trimming bits in two's complement. The step size is approximately 22 mV. Maximum voltage at 0x3. Minimum voltage at 0x4. Changing this parameter is not recommended as it affects waveform amplitude.

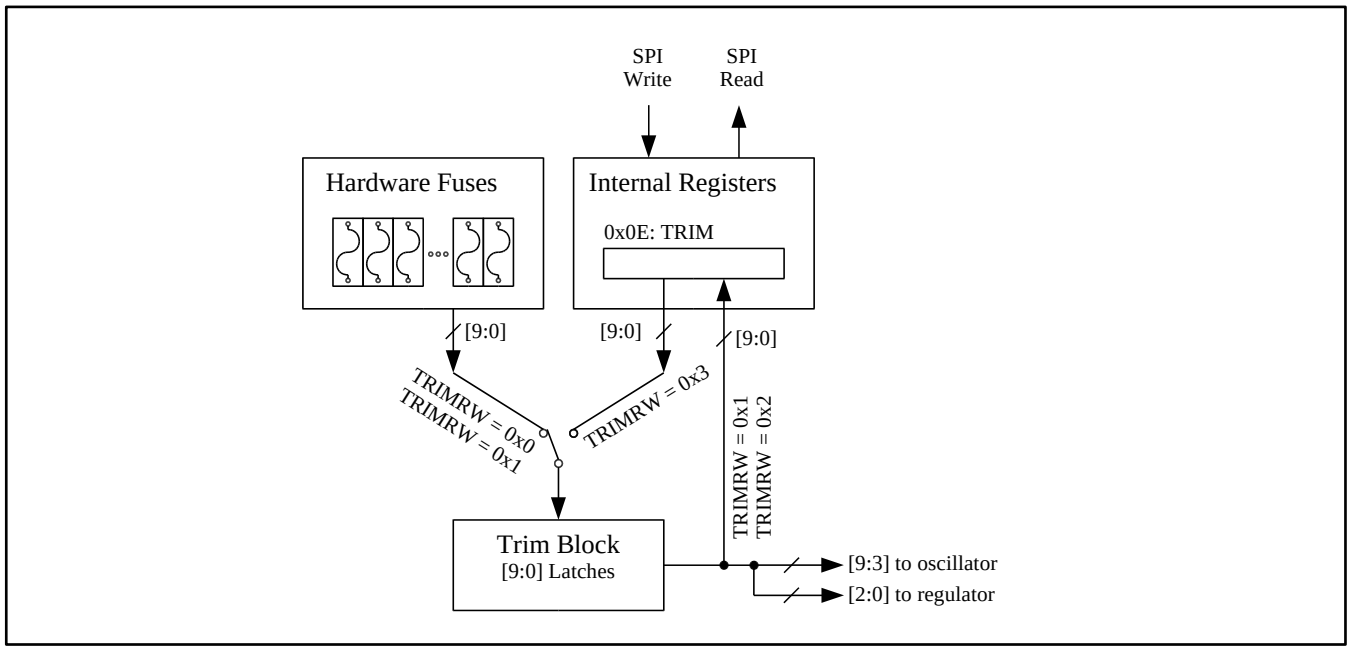


Figure 21: Trim control block diagram

6.11.16 0xF CHIP_ID

Table 43: CHIP_ID register details

ADDRESS: 0xF	CHIP_ID					DEFAULT:0x034					
11	10	9	8	7	6	5	4	3	2	1	0
RSVD						CHIP_ID[5:0]					

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
5:0	CHIP_ID	0x34	R	The field indicates the product revision of the device, as follows: 0x34: Rev. D

6.11.17 SDO Broadcast Details

The internal register whose content is returned to the full-duplex SPI port (SDO pin) is selected by BC[4:0] bits. Note that the SPI transaction to read register content on the SDO pin must be performed at least 400 ns after the BC[4:0] bits are written.

The main register content can be broadcast by setting BC[4:0] bits from 0x00 to 0x0F and the returned 16-bit content is detailed in Table 44.

Extra broadcast registers are also available by setting BC[4:0] bits to 0x10, 0x11, 0x12 and 0x1C, and the returned 16-bit content is detailed in Table 45 to Table 48.

Table 44: BC [4:0] = 0x00 to 0x0F: details of the 16-bit data returned on the SPI port (SDO pin)

BC [4:0] = 0x00 to 0x0F															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BC[3:0]				Content of register with address BC[3:0]											

Table 45: BC [4:0] = 0x10: details of the 16-bit data returned on the SPI port (SDO pin)

BC [4:0] = 0x10															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				STATE[1:0]		VFEEDBACK[9:0]									

BITS	NAME	DESCRIPTION
11:10	STATE	STATE of the controller. 0x0: IDLE 0x1: CALIBRATION 0x2: RUN 0x3: ERROR
9:0	VFEEDBACK	10-bit unsigned value representing the voltage measured on HV pin (V_{HV}). The relation between V_{HV} in volt and VFEEDBACK[9:0] is determined by: $$VFEEDBACK[9:0] = V_{HV} \times 7.68$$

Table 46: BC [4:0] = 0x11: details of the 16-bit data returned on the SPI port (SDO pin)

BC [4:0] = 0x11															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD						OFFSET[9:0]									

BITS	NAME	DESCRIPTION
9:0	OFFSET	10-bit unsigned value representing an internal offset voltage when the voltage across the piezo is 0 V. This value is updated every time OE bit is set to 0x1. The OFFSET[9:0] value varies from chip to chip.

Table 47: BC [4:0] = 0x12: details of the 16-bit data returned on the SPI port (SDO pin)

BC [4:0] = 0x12															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD					SENSE	SENSE_FLAG	SENSE_VALUE[8:0]								

BITS	NAME	DESCRIPTION
10	SENSE	Indicate when the BOS1211 sensing is activated and SENSE bit is set to 0x1. If value is 0x0, then SENSE_FLAG and SENSE_VALUE bits should be ignored. 0x0: Not Sensing 0x1: Sensing
9	SENSE_FLAG	Indicates if SENSE_VALUE[8:0] met the threshold detection conditions. ONCOMP bit must be reset to 0x0 to reset SENSE_FLAG. 0x1: signal above/below threshold 0x0: Nothing detected
8:0	SENSE_VALUE[8:0]	Signed representation of the piezo sensed voltage (*Amplitude*) in volt.

Table 48: BC [4:0] = 0x1C: details of the 16-bit data returned on the SPI port (SDO pin)

BC [4:0] = 0x1C															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM_DATA_RAW[15:0]															

BITS	NAME	DESCRIPTION
15:0	RAM_DATA_RAW	Read the data present in RAM. To be used in conjunction with RAM SYNTHESIS WRITE and FULL_RAM_READ WFS command (see section 6.10).

7 Implementation

7.1 Typical Configuration

This section presents the recommended schematic for a 4 µF load.

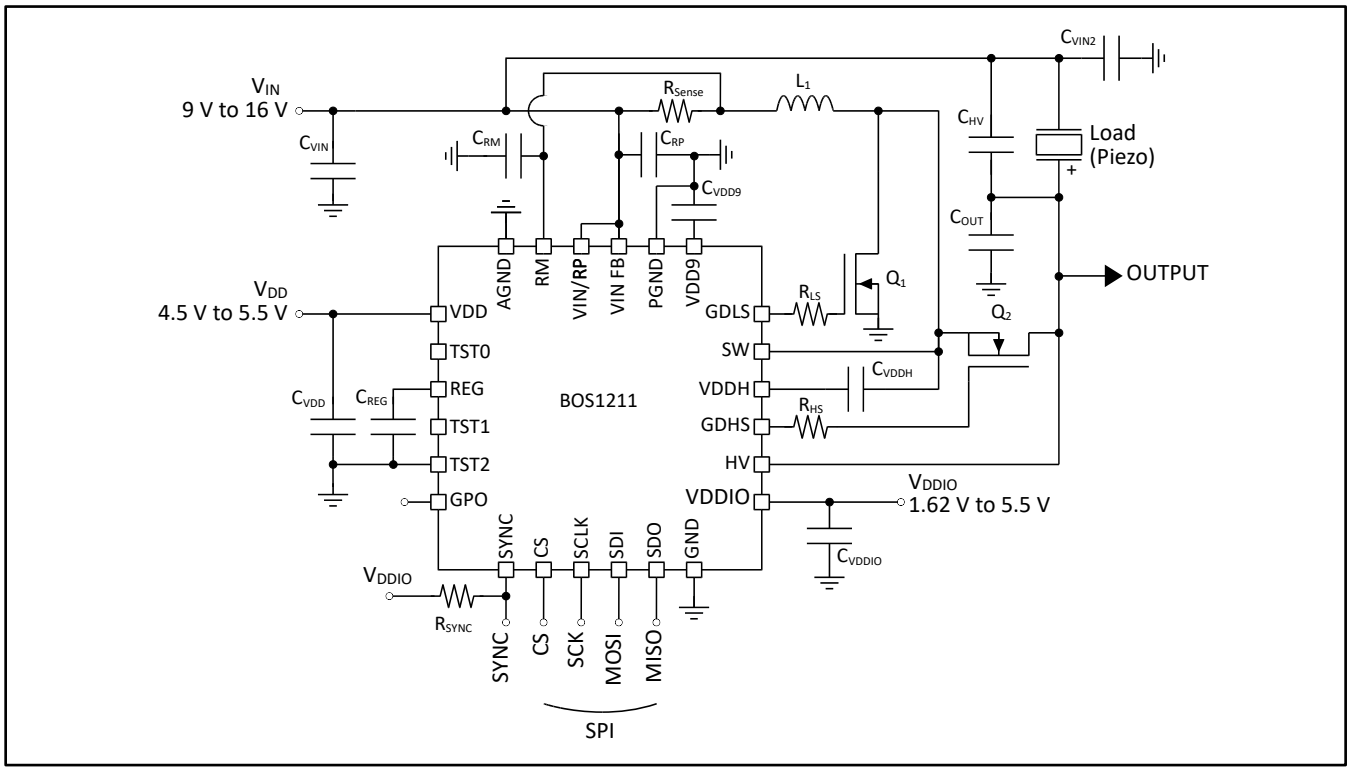


Figure 22: Typical schematic

7.2 External Components

Table 49: Recommended external components for a 4 µF / 120 V load

COMPONENT	DESCRIPTION	TYPICAL VALUE
C_{VIN}	Input capacitor located close to L_1 (1)	22 µF
C_{VIN2}	Input capacitor located close to OUT (2)	330 nF
C_{VDD}	V_{DD} decoupling capacitor	100 nF
C_{VDDIO}	V_{DDIO} decoupling capacitor	100 nF
C_{REG}	Internal regulator decoupling capacitor	100 nF
C_{VDD9}	Internal V_{DD9} capacitor	100 nF
C_{VDDH}	VDDH capacitor	4.7 nF
C_{HV}	Boost capacitor	5% of load
C_{OUT}	OUTPUT capacitor (3)	220 nF
C_{RP}	RP bypass capacitor (optional)	4.7 nF
C_{RM}	RM bypass capacitor (optional)	4.7 nF
R_{sense}	Current sense resistor	39 mΩ, 1 W
R_{SYNC}	SYNC pull-up resistor	10 kΩ
R_{LS}	Q_1 gate series resistance	20 Ω
R_{HS}	Q_2 gate series resistance	20 Ω
L_1	Boost inductor	10 µH
Q_1	Low side NMOS switch	See section 7.4.5
Q_2	High side NMOS switch	

(1) C_{VIN} is the capacitor required to be located close to L_1. Another capacitor may be required. See section 7.4.4 for the total capacitance to put on V_{IN} node.

(2) A second capacitor C_{VIN3} (typically 3.9 nF) & C_{VIN4} (typically 100 nF) can optionally be placed in parallel to improve EMC performances.

(3) A second capacitor C_{OUT2} (typically 3.9 nF) can optionally be placed in parallel to minimize high frequency noise.

7.3 Initialization

7.3.1 Power-Up Sequence

With an active MCU connected to its digital interface, the BOS1211 can be powered on with the following sequence:

1. Apply power to the BOS1211 device. Note that the V_{DD} ramp-up rate should be at least 3V/ms, V_{IN} can be applied before or at the same time as V_{DD}, and V_{DDIO} can be applied at any time.
2. Wait 3 ms for the BOS1211 to start-up with the sequence presented in Figure 23, with the following steps:
    a. V_{DD} Power-up
    b. Device initialization
    c. Device going to SLEEP
3. Wake-up from SLEEP forcing a pulse low on $\overline{CS}$ pin or performing a dummy SPI write.
4. Wait 50 µs for the device to wake-up and enter the IDLE state.
5. Program the desired main registers according to your application.
6. The device is ready for waveform playback.

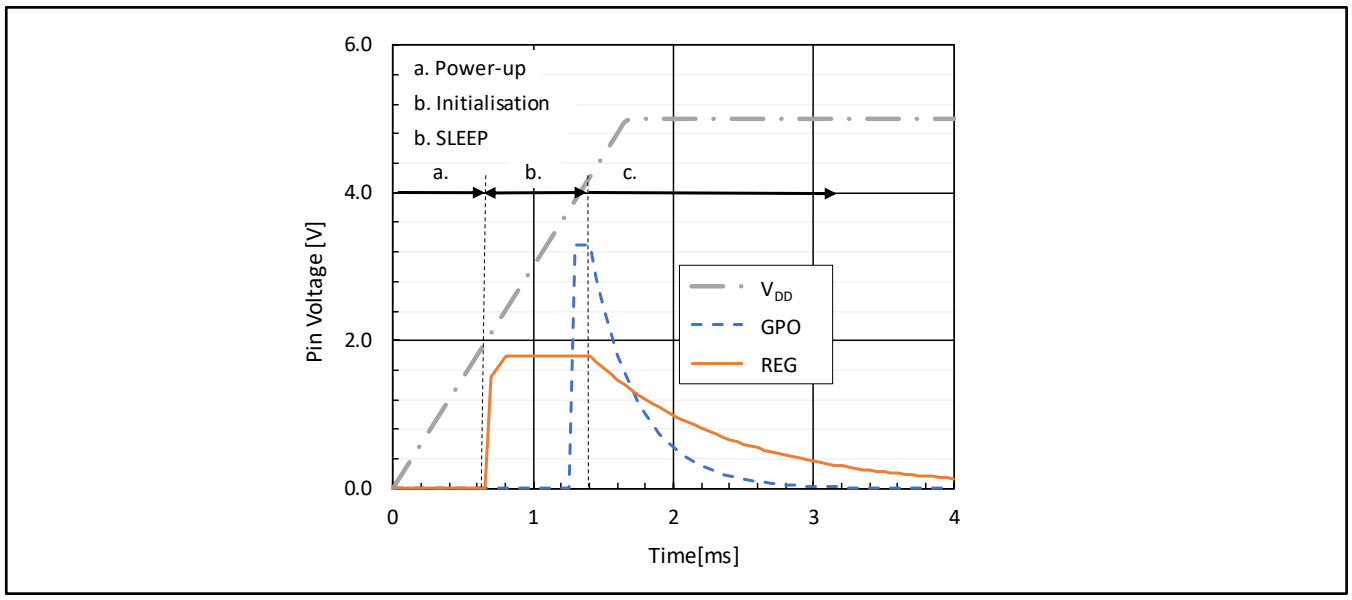


Figure 23: Typical V_{DD}, GPO & REG pin voltage during device initialization

7.3.2 Start-Up Sequence

Once the BOS1211 is powered up, it can wake-up from SLEEP state with the following start-up sequences:

- From SLEEP state, users must perform steps 3 to 7 of section 7.3.1.
- From IDLE state, the device is ready for waveform playback.

7.4 Design Methodology: selection of components

7.4.1 Load Selection

The BOS1211 is designed to drive a load of up to 4 µF at 120 V and 300 Hz. Larger load capacitances (C_{Load}) can be driven if the waveform frequency and/or the waveform amplitude is reduced or if discrete components are scaled appropriately.

Load capacitance defines the required value of component C_{HV} using the following equation:

$$C_{HV} = 5\%\, C_{Load} \quad (1)$$

The capacitor should have a voltage rating at least equivalent to the maximum amplitude of the waveform. For instance, for a 120 V waveform, a capacitor with a minimum voltage rating of 120 V is required.

7.4.2 Inductor Selection

A 10 µH L_1 inductor is recommended but many COTS inductor may be used depending on the application. The peak current required in your design will set the minimum saturation current acceptable for your inductor.

You can use the following procedure to find the L_1 minimum saturation current required:

1. Set the haptic waveform maximum frequency (f_{sig}). e.g., 300 Hz.
2. Set the maximum amplitude of the waveform (V_{pk}). e.g., 120 V
3. Set the minimum supply voltage (V_{IN}) value during operation, e.g., 12 V
4. Calculate the maximum power transfer point with the following equations:

$$V_{OUT} = \frac{V_{pk}}{2}(1 + \sin(30)) + V_{IN} \quad (2)$$

$$\overline{I_{OUT}} = \pi f_{sig} C_{Load} V_{pk} \cos(30) \quad (3)$$

5. Calculate the average input current ($\overline{I_{IN}}$) in amps with the following equation:

$$\overline{I_{IN}} = 1.5 \times \frac{V_{out} \times \overline{I_{out}}}{V_{IN}} \quad (4)$$

6. Calculate the inductor peak current (I_{pk}) in amps using the following equation:

$$I_{pk} = 1.5 \times \overline{I_{IN}} \quad (5)$$

For an optimal design, the inductor with the smallest DCR value possible should be used with saturation current higher than I_{pk}.

7.4.3 Current Limit Selection (R_{sense})

The current limit of the power converter is set by R_{sense}. The value of R_{sense} must be selected to enable a current range appropriate for the I_{pk} value calculated for the inductor (see section 7.4.2). Refer to Table 50 and equation (6) to estimate R_{sense} value. Make sure that the saturation current of the inductor

selected is higher than the current limit. The current limit that will flow passing through R_{sense} in amps is determined by the following equation:

$$\text{Current Limit} = \frac{0.256}{R_{sense}} \quad (6)$$

Table 50: Inductor peak current limit, min/max values

R_{sense} [Ω]	CURRENT LIMIT [A]	COMMENT
1.0	0.256	Maximum R_{sense} value
0.068	3.8	
0.03	8.5	Minimum R_{sense} value

7.4.4 Input Capacitor (C_{VIN})

An input capacitor (C_{VIN}) must be placed next to the inductor because of the current requirement of the power converter. A low-ESR capacitor of at least 10 µF is recommended.

The energy recovered from the load in reverse mode accumulates on C_{VIN} and causes the input voltage to increase. The voltage increase must not make the total voltage on C_{VIN} exceed the 19.9 V limit (V_{IN_max}). Equation (7) helps find the minimum capacitance value for your specific design. The capacitance maybe distributed across the power distribution network on V_{IN}.

$$C_{VIN} = \frac{C_{load} \times V_{pk}^2}{V_{IN\_max}^2 - V_{Supply12V\_max}^2} \quad (7)$$

Where $V_{Supply12V\_max}$ is the maximum voltage expected on the 12 V supply for the application and V_{IN_max} = 19.9 V is the maximum tolerable voltage at VIN/RP pin without triggering a OVLO12 fault. When selecting the capacitor, make sure its effective capacitance is closed to the calculated value in your operating conditions.

7.4.5 External Transistors (Q_1 & Q_2)

The external NMOS transistors must be chosen with the following criteria:

1. Peak drain current greater than I_{pk} when V_{GS} is greater than 6 V.
2. Lowest drain-source resistance (R_{DSON}) possible.
3. The Gate capacitance (C_{ISS}) should be ≤2 nF to have a fast enough rise time of the gate driver output.
4. Drain-source breakdown voltage (BV_{DSS}) greater than V_{pk} + V_{INMAX}.
5. Lowest gate to drain (C_{RSS}) capacitance possible.

7.4.6 VDDH Capacitor (C_{VDDH})

The C_{VDDH} capacitance depends on gate capacitance of Q2 (C_{ISS-Q2}) and must be selected as follows:

$$7 \times C_{ISS-Q2} \leq C_{VDDH} \leq 20 \times C_{ISS-Q2} \quad (8)$$

7.4.7 Validating Component Choice

The MXPWR bit can be monitored to validate that the components choice is performing well in a specific design. A MXPWR bit going to 0x1 means that the peak current calculated is too low and the circuit needs to be modified.

Also note that a higher L_1 inductor DCR and Q_1/Q_2 NMOS R_{DSON} reduce the BOS1211 efficiency and lead to a higher I_{pk} requirement.

Designing a circuit to drive a wide range of piezo OUTPUT voltage may require larger components to accommodate the higher I_{pk} at low voltage. One can consider using a lower haptic waveform amplitude or frequency at lower V_{IN} to reduce the size and cost of the solution.

7.5 Design Methodology: Programming

Many operational settings are adjustable through the digital front end. Users should program the following parameters according to its specific design.

7.5.1 Waveform Playback

- Set FIFO readout speed: CONFIG.PLAY[2:0]

7.5.2 Power Converter

- Set the maximum switching frequency of the power converter: ION_BL.FSWMAX[1:0]
- Set SLS and SHS parameters according to the selected MOS transistors: PARCAP.SLS[1:0], PARCAP.SHS[1:0]

7.5.3 Loop Controller

The BOS1211 implements a proportional-integral (PI) control loop feedback. Users can optimize the following parameters if required:

- Set proportional gain using KP.KP[10:0]
- Set proportional gain term related to waveform amplitude with KPA_KI.KPA[7:0]
- Set integral term KPA_KI.KIBASE[3:0]

Table 51 shows the recommended value for a 4 µF load operating at up to 120 V and 300 Hz with a L_1 = 10 µH and R_{sense} = 39mΩ.

Table 51: Loop controller parameters

PARAMETER	RECOMMENDED VALUE	COMMENT
KP	0x80 (default value)	Reduce value for smaller loads
KPA	0x10 (default value)	Reduce value for smaller loads
KIBASE	0x3 (default value)	Increase value to 3 or 4 when using a larger inductor

7.5.4 Power Efficiency

The power consumption of the BOS1211 and haptic waveform integrity can be optimized by configuring the internal controller and the switching timing of the power MOSFETs. To do so, adjust the following registers based on the selected inductor (L), current sense limit (R_{sense}) and power transistors (Q_1 and Q_2):

- Set proportional gain using KP.KP[10:0]
- Adjust power switch deadtime using DEATIME.DHS[6:0] and DEADTIME.DLS[4:0]
- Adjust low-side and high-side gate drivers strength using PARCAP.SLS[1:0] and PARCAP.SHS[1:0]
- Adjust minimum current required to turn on HS using ION_BL.IONSCALE[7:0]
- Adjust PARCAP.PARCAP[7:0] based on capacitance seen on pin SW
- Adjust proportional gain for the offset using SUP_RISE.TI_RISE[5:0]
- Set the nominal supply voltage (V_{IN}) of the design using SUP_RISE.VIN[4:0]

8 Layout

A 4-layer PCB layout example is presented in Figure 24. The recommended layers are as following:

- Top layer - Components, main routing and V_{IN}.
- Layer 2 - Full ground plane, avoid interruptions/slot as much as possible.
- Layer 3 - Power plane split between V_{DD}, V_{DDIO} and GND.
- Bottom layer - Routing.

Layout considerations:

1. Keep V_{IN} node on the Top layer, using a minimum trace length (avoid the use of a power plane).
2. Keep SW node area as small as possible, the use of a copper region is recommended to increase current capability.
3. Place and route components Q_1, C_{VIN1} to C_{VIN4}, C_{OUT1} and C_{OUT2} with the following considerations:
    a. Place components close to each other to minimize area of the high di/dt current loop and reduce high voltage ringing & spikes.
    b. Force the high current path on the OUT and VIN nodes to flow through the decoupling capacitors C_{VINx} and C_{OUTx} in increasing order of values; the lower value capacitors should be closer to the high di/dt current loop.
    c. Create a GND island on the Top layer connecting to all these components, fill with vias to layer 2 ground plane. This GND island must not be tied to the top layer ground polygon/plane (if applicable).
4. Place C_{HV} between C_{OUT1} and C_{VIN2}.
5. Route Vin/RP & RM sensing lines parallel to each other.
6. Route SW & GDHS lines going to Q_2 in parallel to each other and keep lines length as short as possible (bottom layer).
7. Route VIN-FB & OUT sensing lines parallel to each other and keep lines length as short as possible (bottom layer).

EMI recommendations:

8. Use RHS and RLS resistors of 20 Ω on GDHS and GDLS signals.
9. Use a Common mode choke at the input of V_{IN} and/or at the output if needed.

Notes on important components:

- The layout example is sized for a piezo TDK Powerhap™ actuator with a capacitance in the range of 3 to 4 µF. L_1 inductor and C_{HV} capacitor footprints can be reduced with reduced capacitive load.
- Components packages
  - ✓ Q_1 and Q_2 transistors are surface mount 3.3 × 3.3 mm package.
  - ✓ C_{OUTx} and C_{VIN2} to C_{VIN3} capacitors are 0805 (2012).
  - ✓ C_{VIN1} and CHV capacitors are 1210 (3125).
  - ✓ R_{Sense} resistor is 1206 (3216).

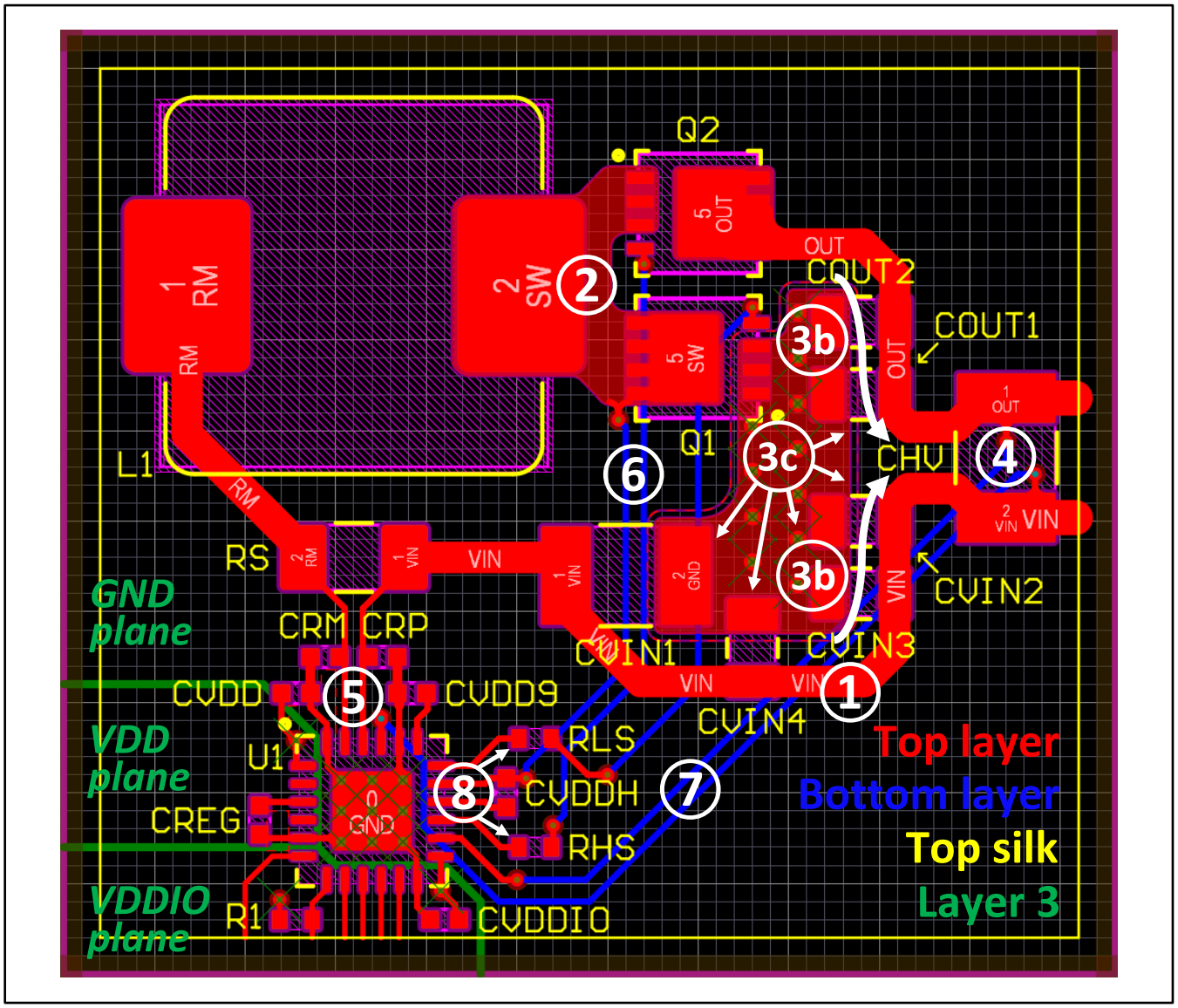


Figure 24: Recommended PCB Layout

9 Mechanical - BOS1211AQ (QFN)

9.1 Package Description

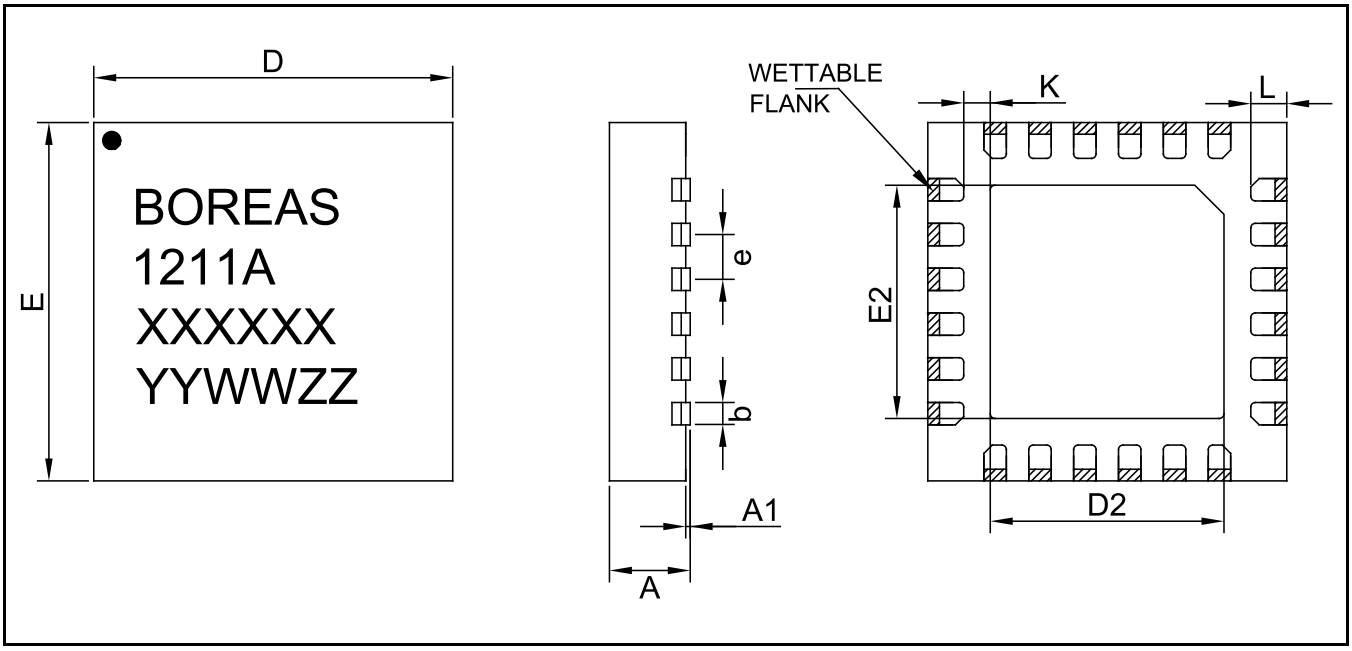


Figure 25: QFN 24L 4.0mm x 4.0mm package outline drawing

Table 52: QFN 24L 4.0mm x 4.00mm package dimensions

SYMBOL	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.025	0.05
b	0.20	0.25	0.30
D		4.00 BSC	
D2	2.45	2.50	2.55
E		4.00 BSC	
E2	2.45	2.50	2.55
e		0.50 BSC	
K	0.17	-	-
L	0.45	0.50	0.55

‡BSC: Basic Spacing between Center
‡‡Reference: JEDEC MO-220-WGGD

Four lines are branded on the package:

(1) Company Name: BOREAS
(2) Device Marking: 1211A
(3) Wafer Batch Number: XXXXXX
(4) Assembly Date Code: YY (Year), WW, (Week) and ZZ (Assembly House)

9.2 Package Soldering Footprint

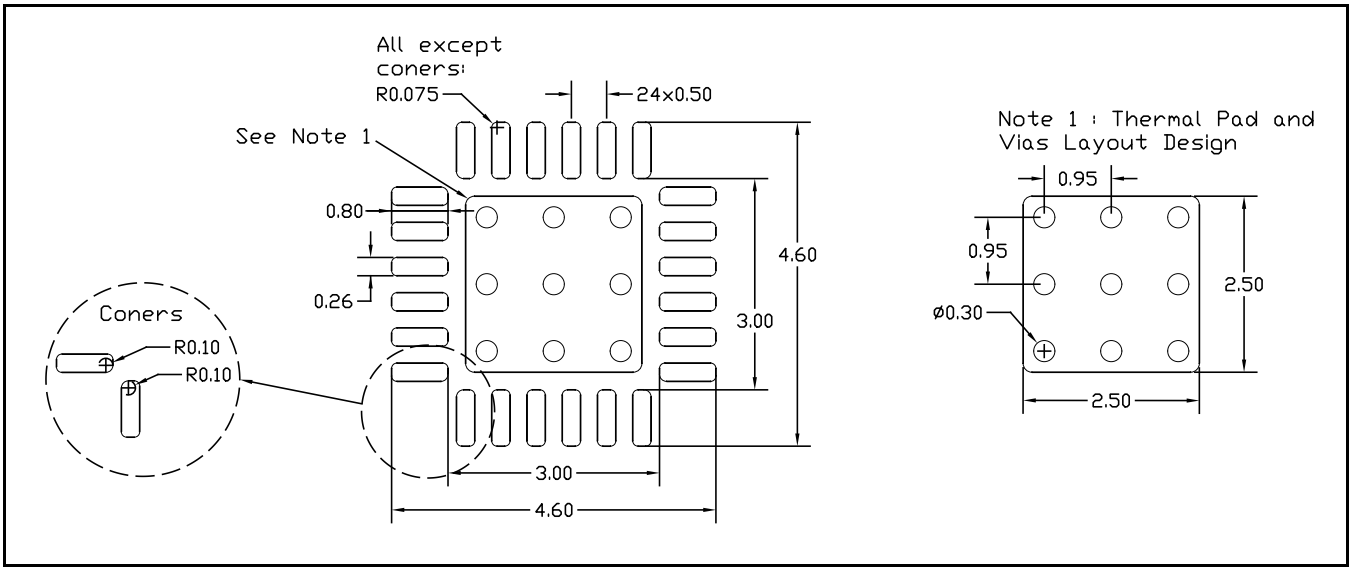


Figure 26: QFN 24L 4.0mm x 4.0mm soldering footprint (NOT TO SCALE)

9.3 QFN Reflow

The QFN package soldering reflow profile should be determined based on the recommended reflow profile made by the manufacturer of the solder paste used. Also, it is important to take into considerations that the circuit board dimensions, other board components and the reflow soldering oven may affect the reflow profile.

Finally, please note that the quality of the solder paste plays an important role in board assembly and allows for a reliable and repeatable assembly process.

9.4 Tape and Reel Specification

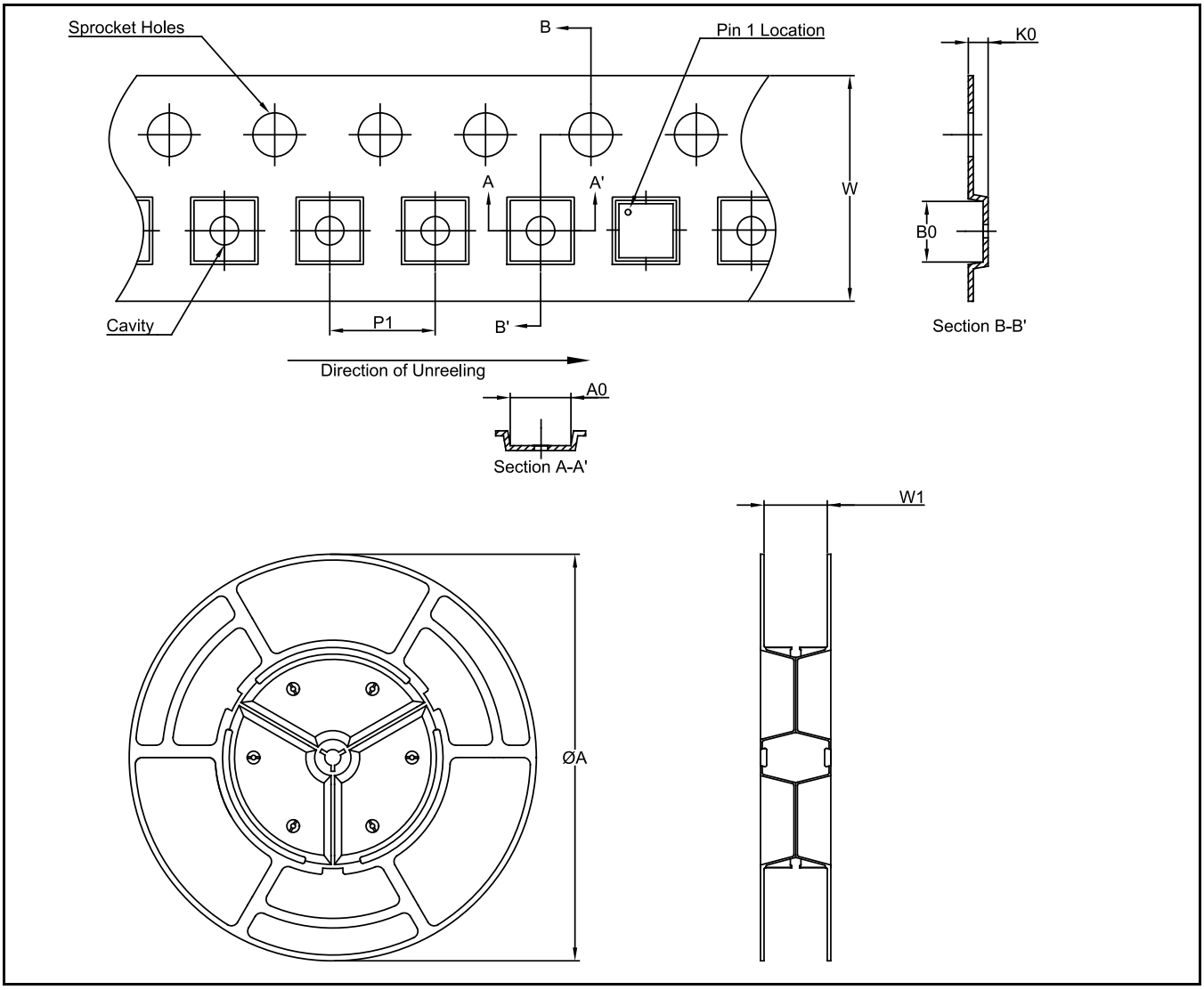


Figure 27: Embossed carrier tape and reel outline (NOT TO SCALE)

Table 53 Tape and reel dimensions

PART NUMBER	PACKAGE TYPE	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W	⌀A (mm)	W1 (mm)
BOS1211AQ	QFN	4.40	4.40	1.80	8.00	16.0	330.0	13.9

10 Ordering Information

Table 54: Ordering information

	ORDERING PART NUMBER (1)	PACKAGE (2)	PACKING FORMAT	QUANTITY (3)	MSL PEAK TEMP. (4)	DEVICE MARKING
1	BOS1211AQR	QFN 24L 4.0mm x 4.0mm	Tape & Reel (R)	2500 / Reel	Level 3 260 °C/168 Hrs	1211A

NOTE

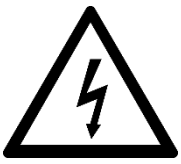
(1) Ordering Part Number where last letter indicates packing format.
(2) All parts are RoHS compliant.
(3) Contact sales@boreas.ca to order.
(4) MSL is the Moisture Sensitivity Levels, IPC/JEDEC J-STD-020.

11 Document History

ISSUE	DATE	DOCUMENT NUMBER	CHANGES
5	March 2024	BT002DDS01.01	Product Datasheet. Updated section 5.3 & 5.4. Added typical performance characteristics (section 5.6). Clarified examples of section 6.5, 6.6, 6.7, 6.8 & 6.9. Added notes to sensing feature (section 6.9). Added CHIP_ID field details (section 6.11.16). Updated power-up sequence (section 7.3.1). Updated layout recommendation (section 8). Updated POD and soldering footprint (section 9.1 & 9.2).
4	January 2022	BT002CDS01.02	Preliminary Datasheet. Improved WFS commands explanation (section 6.9). VDDIO operating conditions widened (section 5.3). Added Tape and Reel information (section 9.4).

12 Notice and Warning

Warning High Voltage



For safety, this integrated circuit must be used by qualified and skilled personnel familiar with all applicable safety standards.

ESD Caution

This integrated circuit is ESD (Electrostatic Discharge) sensitive. Therefore, proper ESD precautions and procedures are recommended for handling and installation to avoid damage.

